Simulation model for routes in public transport systems using parallel computing in IoT environments

Doctoral Thesis

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To my wife Carolina and my son Jacobo

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Abstract

Background

There are a large number of tools for the simulation of traffic and routes, which take into account the different simulation models (macroscopic, microscopic, and mesoscopic). Unfortunately, these simulation tools are limited when simulating a complete public transport system, which includes all its buses and routes (up to 270 for the London Underground). The processing times for this type of simulation increase in an unmanageable way, since all the relevant variables that are required to simulate consistently and reliably the system behavior must be evaluated. Different studies nationwide have encountered this problem. In these, tools have been generated for the simulation and optimal allocation of routes in mass transport systems such as Transmilenio in Bogotá, Colombia, concluding that current simulation models cannot simulate systems of public transport completely. This problem is because they represent a large-scale NP-hard problem, in which the time required for simulation increases exponentially when a new element is added.

At present, the processing capacity of modern computers is no longer measured based on the clock frequency of their CPUs, since the limit allowed by silicon has been reached (around 4GHz). Today the processing capacity depends more on the number of cores and the amount and speed of RAM. Unfortunately, to the date, there are no enough models for the simulation of the behavior of routes in public transport systems that take advantage of the benefits of parallel processing provided by modern computer systems, such as GPUs, or other parallel processing architectures. Therefore, we found that there is a lack of simulation models that can handle the behavior of all routes of a public transport system efficiently and consistently, taking advantage of parallel computing.

Aims

The main aim of this project is the purpose of a new public transport systems' routes simulation model for parallel computing architecture in IoT environments. This aim comprises the following objectives:

- Identify the input and output variables for a routes simulation model in public transport systems, from IoT environments.
- Define a parallel computing architecture that is efficient for the execution of route simulation models in public transport systems.

- Construct a new simulation model for the defined parallel computing architecture, which, through the identified input and output variables, allows the simulation of routes in public transport systems to be carried out efficiently and consistently.
- Validate the consistency of the new simulation model using other simulation models already validated.
- Evaluate the performance of the new simulation model, in contrast to other models executed in different architectures.

Methods

A scientometric tool called ScientoPy was built to support the state of the art analysis. In state of the art, we reviewed the applications for the Internet of Things focusing on Smart Cities and then in Intelligent Transport Systems. Then, we review the applications for the three main parallel processing architectures: GPU, FPGA, and multi-core to find parallel implementations for public transport simulation. Next, a validation public transport simulator was build entirely in Python with dynamic lists to emulate the passengers' queues in the stops and buses. We named this as Pure Python simulator. The behavior of this simulator was validated with the simulation output data consistency and with the graphical real-time 3D output that shows the passengers and buses' movement in the system. Then, we designed and built a parallel simulation model called Masivo PSC (Parallel Simulation Core) then performs concurrently the arrival, boarding, and alighting operations per each stop in a separate work item that runs in OpenCL. Furthermore, we validated the Masivo PSC simulation outputs with the Pure Python simulator outputs for 4 scenarios. Finally, we extracted the simulator performance indicators for the most complicated scenario with 300 stops and near to 500,000 passengers.

Results

In the validation results, we found that the relative error for the total alighted passengers and the total average commute time is not greater than 0.7 % in all of the 4 tested scenarios. The performance results of Masivo show a speed-up factor of 10.2 compared with the simulator model running with one compute unit, and speed-up factor of 278 times faster than the Pure Python validation simulator. The real-time factor achieved was 3050 times faster than the 10 hours simulated duration.

Conclusions

A new simulation model for routes in public transport systems using parallel computing in IoT environments, called Masivo PSC was generated. Masivo works with a predefined public transport system conditions, which include the stops total number, stops' capacity, and the OD matrix. This OD matrix and routes information can be updated to this model via CSV files. Masivo gets the simulation results for total alighted passengers and average commute time. Similarly, it shows the performance indicators.

Keywords:

simulation, parallel, multi-core, public transport, OpenCL.

Resumen

Antecedentes

Hay una gran cantidad de herramientas para la simulación de tráfico y rutas en sistemas de trasnporte público, que tienen en cuenta los diferentes modelos de simulación (macroscópica, microscópica y mesoscópica). Desafortunadamente, estas herramientas de simulación son limitadas cuando se simula un sistema de transporte público completo, que incluye todos sus autobuses y rutas (hasta 270 para el caso del metro de Londres). Los tiempos de procesamiento para este tipo de simulaciónes aumentan de manera inmanejable, ya que todas las variables relevantes que se requieren para simular de manera consistente y confiable el comportamiento del sistema deben ser evaluadas. Diferentes estudios a nivel nacional han encontrado este problema. En estos, se han generado herramientas para la simulación y asignación óptima de rutas en sistemas de transporte masivo como Transmilenio en Bogotá, Colombia, concluyendo que los modelos de simulación actuales no pueden simular completamente los sistemas de transporte público. Este problema se debe a que representan un problema NP-hard a gran escala, en el que el tiempo requerido para la simulación aumenta exponencialmente cuando se agrega un nuevo elemento.

En la actualidad, la capacidad de procesamiento de las computadoras modernas ya no se mide en función de la frecuencia de reloj de sus CPU, ya que se ha alcanzado el límite permitido por el silicio (alrededor de 4 GHz). Desafortunadamente, hasta la fecha, no existen modelos suficientes para la simulación del comportamiento de las rutas en los sistemas de transporte público que aprovechan los beneficios del procesamiento paralelo proporcionado por los sistemas informáticos modernos, como las GPU u otras arquitecturas de procesamiento paralelo. Por lo tanto, descubrimos que faltan modelos de simulación que puedan manejar el comportamiento de todas las rutas de un sistema de transporte público de manera eficiente y consistente, aprovechando la computación paralela.

Objetivos

El objetivo principal de este proyecto proponer un nuevo modelo de simulación de rutas en sistemas de transporte público para una arquitectura de computación paralela, en entornos IoT. Este objetivo comprende los siguientes objetivos:

- Identificar las variables de entrada y salida para un modelo de simulación de rutas en sistemas de transporte publico, desde los entornos IoT.
- Definir una arquitectura de computación paralela que sea eficiente para la ejecución de modelos de simulación de rutas en sistemas de transporte público.

- Construir un nuevo modelo de simulación para la arquitectura de computación paralela definida, que mediante las variables de entrada y salida identificadas, permita realizar de manera eficiente y consistente la simulación de rutas en sistemas de transporte público.
- Validar la consistencia del nuevo modelo de simulación mediante otros modelos de simulación ya validados.
- Evaluar el rendimiento del nuevo modelo de simulación, en contraste con otros modelos ejecutados en diferentes arquitecturas.

Métodos

Se creó una herramienta cienciométrica llamada ScientoPy para soportar el análisis del estado del arte. En este estado del arte, revisamos las aplicaciones para el Internet de las cosas centrándose en las ciudades inteligentes y luego en los sistemas inteligentes de transporte. Luego, revisamos las aplicaciones para las tres arquitecturas principales de procesamiento paralelo: GPU, FPGA y multi-core para encontrar implementaciones para la simulación del transporte público. A continuación, se construyó un simulador de transporte público de validación completamente en Python con listas dinámicas para emular las colas de los pasajeros en las paradas y autobuses. A este simulador lo denominamos Pure Python simulator. El comportamiento de este simulador se validó con la consistencia de los datos de salida de la simulación y con la salida gráfica en 3D en tiempo real que muestra el movimiento de los pasajeros y autobuses en el sistema. Luego, diseñamos y construimos un modelo de simulación paralela llamado Masivo PSC (Parallel Simulation Core) que ejecuta en paralelo las operaciones de llegada, embarque y desembarque por cada parada en un work-item independiente que se ejecuta en OpenCL. Además, validamos los resultados de la simulación de Masivo PSC con los resultados del simulador Pure Python para 4 diferentes escenarios. Finalmente, extrajimos los indicadores de rendimiento del simulador para el escenario más complicado con 300 paradas y cerca de 500,000 pasajeros.

Resultados

En los resultados de la validación, encontramos que el error relativo para el total de pasajeros desembarcados y el tiempo de viaje promedio total no es mayor que el 0.7 % en los 4 escenarios probados. Los resultados de rendimiento de Masivo muestran un speed up factor de 10.2 comparado con el mismo ejecutado en una sola unidad de cómputo, y un speed up factor de 278 veces más rápido que el simulador de validación Pure Python. El real-time factor alcanzado fue de 3050 veces más rápido que el tiempo total simulado de 10 horas.

Conclusiones

Se generó un nuevo modelo de simulación para rutas en sistemas de transporte público que usa computación paralela en entornos IoT, llamado Masivo PSC. Masivo trabaja con un sistema de transporte público predefinido, que incluye el número total de paradas, la capacidad de las paradas y la matriz de origen-destino.

Palabras clave:

simulación, paralelo, multi-core, transporte público, OpenCL.

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Chapter 1

Introduction

1.1 Problem statement

The Internet of Things (IoT) allows to obtain a true picture of the behavior of a system [1]. Public transport systems are no the exception. For example, in the city of Bogotá - Colombia, Transmilenio BRT (Bus Rapid Transit) and the regular buses total more than 8,825 vehicles [2, 3]. This fleet currently has a communication system, which sends relevant information of the operation of the system to the operation center, such as: speed, location and route of each of the buses [4]. Other transport systems use vehicle identification technologies with Bluetooth, which allows to the users' mobile devices to have the ability to identify the bus and the route that it is currently in, to send speed and position information of the same route to an operation center [5]. These communication technologies allow each of the buses in a transport system to become an IoT element, putting into practice the concept of the Internet of Vehicles [6]. In this way, the set of these connected vehicles delivers information that allows to infer the behavior of the system. However, despite the rise of scientific technologies and publications in the IoT, to date there is no bibliographic review article that summarizes all the benefits of the IoT to determine the behavior of a public transport system. This information on the behavior of a public transport system is what feeds the bus route and frequency simulation modules, so that, through this simulation, optimize the variables that influence its behavior.

On the other hand, traffic simulation is widely used in research for modeling public transport systems, while allowing the development and planning of their networks [7]. These simulations are based on different models, where they aim to be a representation of the transport system, incorporating the changes that it has in a variant time [8]. For traffic simulation there are three different types of models: macroscopic, microscopic or mesoscopic [9]. In macroscopic simulation models, traffic tends to be simulated as a continuous flow, sometimes using hydraulic flow theories, without individually considering vehicles or passengers [9–11]. On the other hand, microscopic models describe the behavior of the entities that make up the traffic flow (vehicles), as well as their interactions in detail [12, 13]. For their part, the mesoscopic models mix elements of the macroscopic and microscopic models in a single approach, describing the traffic entities from a high level and their behavior and interactions from a lower level [12, 14]. In the case of public transport, a simulation model must have the ability to include at least the following variables:

- Passenger demand (origin - destination matrices) [15–17]
- Bus capacity [18].
- Bus position and speed [19–25]
- Capacity of stations [26, 27]
- Frequency, stops and routes' stop table [28–32]

There are a large number of tools for the simulation of traffic and routes [7, 9, 11, 12, 33–37] which take into account the different simulation models (macroscopic, microscopic and mesoscopic). Unfortunately, these simulation tools are limited when simulating a complete public transport system, which includes all its buses and routes. The processing times for this type of simulation increase in an unmanageable way, since all the relevant variables that are required to simulate in a consistent and reliable way the system behavior must be evaluated. Different studies nationwide have encountered this problem. In these, tools have been generated for the simulation and optimal allocation of routes in mass transport systems such as Transmilenio [38–42], concluding that current simulation models do not have the capacity to simulate systems of public transport completely. This is because they represent a large-scale NP-hard problem [39], in which the time required for simulation increases exponentially as a new element [38,41] is added, where the behavior of each route or stop added to the system, affects the behavior of all the elements already present. For example, if you have a circular route (which runs the same route in both directions) R_1 that must meet the demand for passengers from two stops P_1 and P_2 (see Figure 1.1a), in the simulation model, the demand for passengers at the stop P_1 will vary according to the time (peak hour and valley time), but it also depends on the number of passengers that the route R_1 picks up at that point. However, if a P_3 stop and a R_2 route that runs the P_1, P_3 and P_2 stops are added to the system (see Figure 1.1b); The demand of the P_1 stop now depends on the passengers collected on the routes R_1 and R_2. Likewise, if 5 stops and 4 more routes are added (see Figure 1.1c), the demand for passengers now at the stop P_1 will depend directly on the routes R_1, R_2, R_3 and R_4, which in its route pick up passengers at that stop. In addition, this demand at P_1 will indirectly depend on the new stops where the routes R_1, R_2, R_3 and R_4 pick up passengers, because the bus capacity of the route that passes for P_1 depends on the number of passengers it has collected in the previous stops. For example, if there is a high demand at the P_8 stop, which fills the R_1 route, this route will not be able to pick up passengers at the P_1 stop.

Thus, to consistently simulate the behavior of routes in a complete public transport system, the interaction of each of its elements must be taken into account. Hence, simulation models that have an appropriate performance are required to face this task. Accordingly, the performance of simulation models is measured by the speed it takes to run a simulation. This performance can be measured using two different measures of effectiveness [43]. The first is the Real-time factor, which establishes the relative speed of the simulation with respect to real time. For instance, a real time-factor of 5 means that the simulation runs 5 times faster than real time. The second measure of efficiency is called the speed-up factor, which measures the simulation performance in parallel, revealing the impact of using more than one processor [43].

At present, the processing capacity of modern computers is no longer measured based on the clock frequency of their CPUs, since the limit allowed by silicon has been reached (around

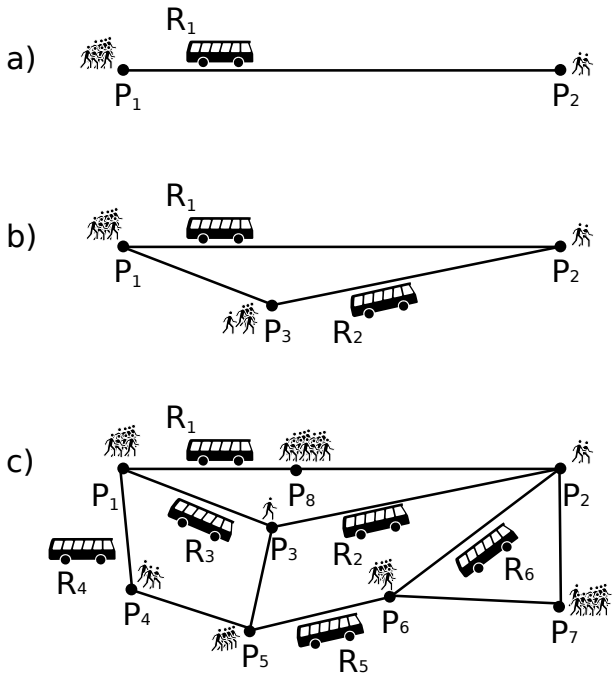


Figure 1.1: Problem of multiple routes and stops. a) 1 route, 2 stops. b) 2 routes, 3 stops. c) 6 routes, 8 stops.

4GHz) [44]. Today the processing capacity depends more on the number of cores and the amount and speed of RAM. For this reason, for tasks that require high computing power, such as graphic processing, graphic processing cards (Graphic Processor Unit - GPU) have increased their number of processing units to more than 1000 cores, also increasing the bandwidth of its memory, thus obtaining a computing power much greater than that of the CPU [45]. This new computing power has been exploited by the scientific community in different types of simulations, such as: urban growth [46], material simulations [47], planetary systems [48], and even traffic simulations [49], among others. Unfortunately, to date there are no models for the simulation of the behavior of routes in public transport systems that take advantage of the benefits of parallel processing provided by modern computer systems, such as GPUs, or other parallel processing architectures.

Therefore, it is concluded that there is a lack of simulation models that have the capacity to handle the behavior of all routes of a public transport system in an efficient and consistent manner, taking advantage of parallel computing.

1.2 Objectives

1.2.1 General Objective

Propose a new public transport systems' routes simulation model for parallel computing architecture, in IoT environments.

1.2.2 Specific Objectives

- Identify the input and output variables for a routes simulation model in public transport systems, from IoT environments.
- Define a parallel computing architecture that is efficient for the execution of route simulation models in public transport systems.
- Construct a new simulation model for the defined parallel computing architecture, which, through the identified input and output variables, allows the simulation of routes in public transport systems to be carried out efficiently and consistently.
- Validate the consistency of the new simulation model using other simulation models already validated.
- Evaluate the performance of the new simulation model, in contrast to other models executed in different architectures.

Chapter 2

State of the art

In this chapter we describe the current level development of the driving technologies for the Internet of Things applications related to urban transportation, parallel processing architectures applications, and parallel public transport simulation. First, we describe the used methodology based in the developed scientometric application called ScientoPy, by described the result published in [50]. Secondly, we present a review of the Internet of Things applications, focused in trending and urban transportation applications, based on the results published in [51]. Next, we include a review of FPGAs' applications and implementations based on the results published in [52]. Then, we summarize the application related to parallel processing in GPU and multi-core architectures, focusing in simulation applications. And finally we discuss the span of the traffic and public transit simulation applications that uses the described parallel architectures.

2.1 Methodology based on ScientoPy scientometric analysis

Scientometric is the study of measuring research quality and impact, understanding the processes of citations, scientific mapping fields, and the use of indicators in research policy and management [53]. Nowadays, we can find a broad range of scientometrics tools: SciMAT [54], Bibexcel [55], CiteSpace [56], CoPalRed [57], Network Workbench Publish or Perish [58], Bibliometrix [59], and others. Most of these tools are specialized in science mapping, that aims to build bibliometric maps that describe how research fields are structured and connected through a network representation [60]. Others tools are specialized in temporal analysis, which aims to identify the nature of phenomena represented by a sequence of observations across different periods of times.

The scientometric analysis shows the topics inside a search criterion, for example, the top countries evolution inside the criterion countries, or a list of specific author keywords inside the criterion author keywords. The temporal analysis allows us to find when a new phenom starts, and when it advances to a trending or emerging topic. The scientometrics tools have developed a kind of algorithms to perform the temporal analysis and find the trending topics, such as strategic diagrams [54, 61] and Kleinberg's burst detection algorithm [56, 62]. These kinds of analysis are performed in datasets that generally are extracted from a single bibliometric database, like Scopus or WoS, because, most of the tools can not merge the information successfully from different databases. Also, there is not a longitudinal graph representation of the trending topics evolution provided by all the actual tools.

In this article, we present a new open-source[1] scientometric tool called ScientoPy. This tool is a Python script based tool specialized in the temporal scientometric analysis. The full source code, instructions manual, and example commands are available in the public repository:
`https://github.com/jpruiz84/ScientoPy`,
and `https://github.com/jpruiz84/ScientoPyUI` for the user interface. Moreover, the tool described here has the following main characteristics:

- Import Clarivate Web of Science (WoS) and Scopus datasets
- Filter publications by document type
- Merge WoS and Scopus datasets based on a field tags correlation table
- Find and remove duplicated documents
- H-index extraction for the analyzed topics
- Country and institution extraction from author affiliations
- Top authors, countries, or institutions extraction based on the first document's authors or all document's authors
- Preprocessing brief graph and report table
- Top topics and specific topics analysis
- Wildcard topics search

[1] With MIT license (for more information, see https://opensource.org/licenses/MIT).

- Absolute and relative growth indications
- Trending topics using the top average growth rate (AGR)
- Five different visualization graphs: timeline, bar, bar trends, evolution, and word cloud
- Command line and graphical user interfaces.

2.1.1 Methodology

In this section, we describe all of ScientoPy's capabilities for scientometric analysis. Figure 2.1 briefs the ScientoPy workflow steps for this kind of analysis. The first step is the input dataset extraction, where we explain which kind of databases and datasets are supported by ScientoPy. Second, the preprocessing that improves the dataset readability and precision, which includes document type filter, field tags correlation, author's name normalization, duplicated removal, times cited, and country/institution extraction. The preprocess results are summarized by the preprocessing brief graph and the preprocessing brief table. Third, in the data analysis, we can perform different operations to extract the top topics, specific topics trends, topic search based on wildcards, or trending topics, inside a selected criterion field (author names, country, author keywords, etc.). Finally, in the visualization step, we can observe the results that we have obtained from the data analysis step, using various graph types such as timeline graph, bar graph, evolution graph, and word cloud.

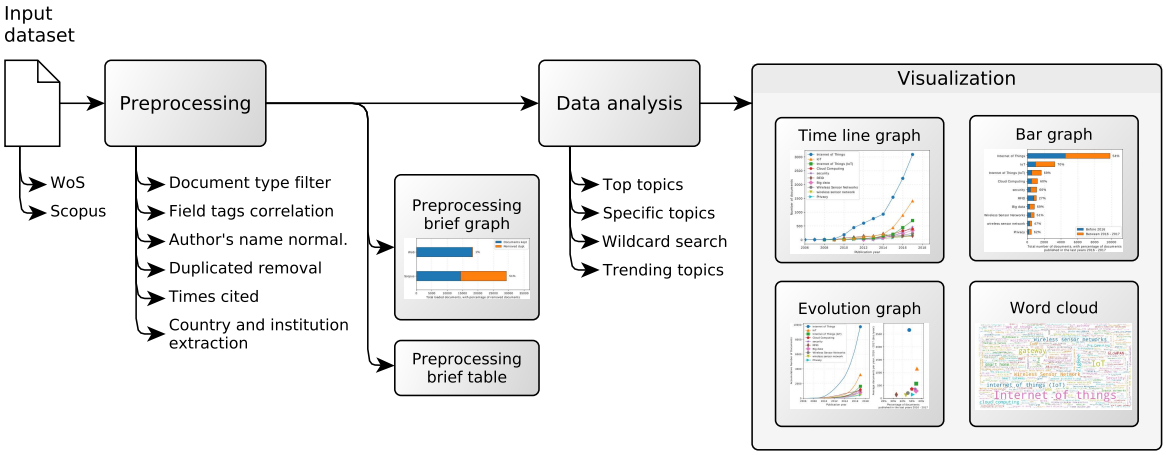


Figure 2.1: ScientoPy scientometrics analysis workflow steps

Dataset extraction

ScientoPy can process datasets from the two main bibliographic databases: Clarivate Web of Science (WoS), and Scopus. For WoS the supported format is *Tab-delimited (Win, UTF-8)*, which can be selected through the export option *Save to Other File Formats*. Also, we recommend saving the *Full Record* option in *Record Content*, to get the full document's information related to authors corresponding address used after for country and institution analysis. On the other

hand, to get the dataset from Scopus, on the Scopus's *Export document settings* section (as the method of export) we must use *CSV Excel*. Then, on the information that we want to export, we select *Citation information*, *Bibliographical information*, and *Abstract & keywords* options. Now, we put all dataset files extracted in a single folder so that ScientoPy preprocessing script can handle them. More detailed instructions to get the dataset is available in ScientoPy's user manual from the public repository.

Preprocessing

ScientoPy uses the preprocessing steps techniques to improve the analysis readability and precision. The following subsections describe these techniques.

Document type filtering By default, ScientoPy filters publications which are classified in one or more of the following document types:

- Conference Paper
- Article
- Review
- Proceedings Paper
- Article in Press

Because this kind of documents represent research works with a higher SJR (SCImago Journal Rank) and JCR (Journal Citation Reports) indicators. Others documents, such as book chapters, short surveys, letters, notes, books, editorials, erratum, reports, retracted documents, meeting abstracts, corrections, software reviews, and hardware reviews are excluded. Nevertheless, by modifying the ScientoPy global settings file, we can customize this document type filter.

Field tags correlation WoS and Scopus use different field tags for their exported datasets. WoS uses two-character field tags, and Scopus uses a full sentence to describe each field. Table 2.1 describes the correlation that ScientoPy uses to convert the WoS to Scopus style fields. Moreover, ScientoPy uses Scopus style to handle and save the preprocessed dataset.

Table 2.1: WoS and Scopus correlation field tags

WoS field tags	Scopus field tags
AU	Authors
BE	Editors
TI	Title
SO	Source Title
LA	Language of original document
DT	Document type
DE	Author keywords
ID	Index keywords
AB	Abstract
C1	Affiliations
EM	Correspondence address
OI	ORCID
CR	Cited references
Z9	Cited by
PU	Publisher
SN	ISSN
BN	ISBN
J9	Abbreviated source title
PY	Year
VL	Volume
IS	Issue
BP	Page start
EP	Page end
AR	Article Number
DI	DOI
PG	Page count
SC	Subject
UT	EID
PM	PubMed ID

Author's name normalization To have coherence in the document's author names, these fields must have consistency between the two input databases, for that reason a author names normalization is need here. For this case, WoS and Scopus have the following inconsistencies in the author's names:

- Scopus uses one comma to divide the authors, and WoS uses a semicolon.
- Scopus uses one dot after the first name initial, and WoS does not.

- WoS uses one comma to separate the author's last name and author's first name initial.
- Some journals use the author name with accents marks, special characters, and others do not.

For instance, Table 2.2 shows two documents original author's names extracted from WoS and Scopus. Here, we observe the differences described previously.

Table 2.2: Two documents author's names fields example from WoS and Scopus ([63, 64]).

Database	Original author's names	Normalized author's names
WoS	Munoz-Organero, M; Ramirez, GA; ...	Munoz-Organero M; Ramirez GA; ...
Scopus	Muñoz-Organero M., Ramírez G.A., ...	Munoz-Organero M; Ramirez GA; ...
WoS	Ciftler, BS; Kadri, A; Guvenc, I	Ciftler BS; Kadri A; Guvenc I
Scopus	Çiftler B.S., Kadri A., Güvenç I.	Ciftler BS; Kadri A; Guvenc I

These author's name inconsistencies generate problems to find similar author's names. For that reason, ScientoPy preprocessing script applies, in this order, the following steps to normalize author's name fields:

1. For Scopus replace the dot and coma (.,) with a semicolon (;)
2. For WoS and Scopus remove dots and comma
3. For WoS and Scopus remove accents marks

Table 2.2 in the third column shows the author's names normalized. Here, we find that the author's names of the same document in the two databases match.

Duplicated removal Duplication removal is a critical step during the preprocessing procedure. If a dataset has duplicated items, the analysis scripts give us results that are not consistent and reliable. This duplication removal filter is based in the DOI and on the document's normalized title and first author last name. For the document title, unfortunately, for some documents that the original language is not English, Scopus adds the original title in square brackets, after the English title, and WoS does not. For instance, Table 2.3 shows two documents that are duplicated on WoS and Scopus with a different title. To solve this problem, for duplication removal, the ScientoPy's preprocessing script normalizes the title by removing the square brackets and the text inside them from the tile and converts it to upper case. In the case of authors name, the first author last name is normalized by removing the accents marks, special characters, and converting it to upper case.

Table 2.3: Document's titles examples from WoS and Scopus ([65, 66]) with the original language name in square brackets

Database	Language	Title
WoS	Turkey	An Overview of oneM2M Standard
Scopus	Turkey	An overview of oneM2M standard [oneM2M Standardina Genel Bir Bakis]
WoS	France	e-Health - The internet of things and telemedicine
Scopus	France	E-Health - The internet of things and telemedicine [E-santé - Objets ...]

Once ScientoPy normalizes the document's titles and first author last name, it runs the steps described on Algorithm 1 for duplication removal. Here, the documents are sorted by the database with WoS first than Scopus. Then, this script sorts the documents by the normalized title. In that way, the documents (before the for loop) are sorted first by the normalized title, and then by the database. In the for loop, ScientoPy processes each document of the documents list. Here, the document DOI, the normalized title, and the normalized first author last name are extracted from the actual processed document by the for loop ($D_{doi[i]}$, $D_{t[i]}$, and $D_{fa[i]}$), and for the document of the next for loop iteration ($D_{doi[i+1]}$, $D_{t[i+1]}$ and $D_{fa[i+1]}$). Because, the documents are sorted by title if there is a duplicated document, the DIOs match, or the normalized title and the normalized first author last name match between two consecutive documents. If two documents match in the for loop iteration, the document of the next iteration is removed from the document list. For the case, if there were two documents from different databases, the Scopus document is removed, because, they were sorted secondly by the database, with WoS document first.

Algorithm 1 Duplicate removal algorithm

```
1: procedure RemoveDuplicates(documentList)
2:     Sort documentList by database, first WoS than Scopus
3:     Sort documentList by normalized title
4:     for each item D in documentList do
5:         D_dio[i] ← D document DIO
6:         D_t[i] ← D title normalized
7:         D_fa[i] ← D first author last name normalized
8:
9:         D_dio[i+1] ← Next D document DIO
10:        D_t[i+1] ← Next D title normalized
11:        D_fa[i+1] ← Next D first author last name normalized
12:
13:        if D_doi[i] == D_doi[i+1] OR (D_t[i] == D_t[i+1] AND D_fa[i] == D_fa[i+1]) then
14:            Get the average times cited between D_[i] and D_[i+1]
15:            Set the average times cited to D_[i]
16:            Remove D_[i+i] from documentList
17:        end if
18:    end for
19:    return documentList
20: end procedure
```

Times cited Scopus and WoS databases report their *time cited* count or cited by number for each document. When a document is duplicated, most of the time, the *times cited* field does not match. For these cases, ScientoPy gets the average **times cited** between the two duplicated documents and sets it in the document that is going to keep (see Algorithm 1, lines 14 and 15). Using this *times cited* field, ScientoPy calculates the h-index of each topic for the different categories, such as authors, countries, institutions, and others.

Document's country To get the document's countries, ScientoPy extracts it from all author's affiliations (last section after the comma of this field). Thus, each document could have one country or many countries associated with it. Nevertheless, if two or more authors have the same country on the affiliation, ScientoPy only associates that country once to the document, to avoid countries duplication per document, and in that way, a document can not add more than once the same country to ScientoPy analysis calculations. For normalization, ScientoPy removes the dot or dots in the country field. Furthermore, some authors use different naming to refer to the same country (such as USA and United States). For that reason, some country names were replaced based on Table 2.4.

Table 2.4: Document's countries names replacing the table. If the original country name meets the criteria, it is replaced. For *equal to country* criterion, the original country field is replaced only if it is equal to the comparison string. For *in country* criterion, the original country is replaced if the comparison string is in the original country field.

Comparison string	Criterion	Replaced to
"Bosnia & Herceg"	Equal to country	Bosnia and Herzegovina
"China"	In country	China
"England" OR "Scotland" OR "Wales"	In country	United Kingdom
"Kingdom of Saudi Arabia"	Equal to country	Saudi Arabia
"Russia"	In country	Russian Federation
"Trinid & Tobago"	Equal to country	Trinidad and Tobago
"U Arab Emirates"	Equal to country	United Arab Emirates
"UK"	Equal to country	United Kingdom
"USA"	In country	United States
"Viet Nam"	Equal to country	Vietnam

For the match criterion *Equal to country*, ScientoPy replaces the original country field only if it is equal to the comparison string. On the other hand, for the match criterion *In country*, the original country is replaced if the comparison string is in the original country field like an asterisk surrounds the comparison string in a wildcard based search. For instance, "TX 77843 USA" is replaced by United States, and "Peoples R China" or "People's Republic of China" are replaced to China.

Document's institutions The document's institutions, are extracted only from all WoS documents author's affiliation fields (first section before comma of this field), because two problems where found in Scopus documents affiliations related to institutions: this field is not always in the same position, and sometimes it is written in the author country's language in Scopus dataset (see Table 2.5). As country, each document could have one institution or many institutions associated with it. Nevertheless, if two or more authors have the same institution on the affiliation, ScientoPy only associates that institution once in the document, to avoid institutions duplication per document, and in that way, an institution can not add more than once the same institution to ScientoPy analysis calculations.

Table 2.5: Document's affiliation examples from WoS and Scopus ([51, 67–69]). Institutions underlined to show that Scopus affiliation not always put it on the same position, and in English

Source	Affiliations
WoS	Sejong Univ, Dept Informat & Commun Engn, Seoul 05006, South Korea
Scopus	Department of Information and Communication Engineering, Sejong University, Seoul, South Korea
WoS	Tokyo Univ Agr & Technol, Tokyo, Japan
Scopus	Tokyo University of Agriculture and Technology, Tokyo, Japan
WoS	Univ Cauca, Dept Telemat, Popayan 190002, Cauca, Colombia
Scopus	Departamento de Telemática, Universidad del Cauca, Popayán, Cauca, Colombia
WoS	Univ Calabria, DIMES, I-87036 Arcavacata Di Rende, CS, Italy
Scopus	DIMES, Università della Calabria, Via P. Bucci, cubo 41C, Rende (CS), Italy

Data analysis

ScientoPy can perform different types of data analysis, including top topics finding and evolution, specific topic evolution, wildcard search, and trending topics. We describe these analysis types below.

Top and specific topics One of the main ScientoPy capabilities is to extract the top topics of a selected criterion. Top topics are the ones that have more documents count in the processed dataset. Table 2.6 shows the criterion options available on ScientoPy. By default, the top topic analysis extracts the 10 top topics on the default criterion (author keywords), and graphs the documents count per topic in horizontal bars. Similarly, we can perform this analysis with specific topics inside a selected criterion. For example, we can compare the documents growth of two specific countries, or the evolution of two different technologies by the author keywords.

Table 2.6: ScientoPy criteria description

Criterion	Description
author	Authors last name and first name initial
sourceTitle	Journal name
subject	Research area (only from WoS documents)
abstract	Document's abstract
authorKeywords	Author's keywords
indexKeywords	Keywords generated by the index. From WoS {Keyword Plus}, and from Scopus {Indexed keywords}
bothKeywords	AuthorKeywords and indexKeywords are used for this search
documentType	Type of document
dataBase	Database where the document was extracted (WoS or Scopus)
country	Country extracted from authors affiliations
institution	Institution extracted from authors affiliations (only from WoS documents)

Moreover, some documents criterion have multiple items. Like a document with multiple authors has multiple author's names and multiple author's affiliations. When we use ScientoPy to extract the top topics inside a criterion, it uses by default the multiple document's fields to calculate the topic count. For example, to extract the top authors, ScientoPy uses all authors of each paper to extract the total top author's list. Similarly, it uses all document's fields inside the topics that could have more than one item, such as authors names, authorKeywords, indexKeywords, bothKeywords, countries, and institutions. Nevertheless, if we want that ScientoPy only uses the first item in the selected criterion to extract the top topics, we can do this by a command option described in the user manual (–onlyFirst command option). In this case, for instance, ScientoPy uses only the first author to extract the top author's list of the dataset.

Wildcard search Wildcards are very useful to find topics that come in plural and singular, such as network and networks. Also, they are effective to find topics inside some defined categories that starts or ends with certain words or phrases, such as:

- *** latency:** operational latency, mechanical latency, WAN latency.
- **blood *:** blood pressure, blood glucose, blood platelets.

For that reason, in the topic analysis, we can use the asterisk (*) wildcard to find, for example, the distribution of the keywords that starts or ends with a particular word or phrase. Also, with this characteristic, we can use ScientoPy to find the documents that in the abstract contain that particular word or phrase.

Topics growth indicators ScientoPy uses three different topic growth indicators to find trending topics and its relative/absolute growth.

Average Growth Rate (AGR) ScientoPy finds the top trending topics based on the higher average growth rate (AGR). The AGR is the average difference between the number of documents published in one year with the number of documents published in the previous year. It indicates how the number of documents published for a topic has growth (positive number) or decline (negative number) on average inside a time frame. This AGR is calculated using the Equation 2.1:

$$AGR = \frac{\sum_{i=Y_s}^{Y_e} P_i - P_{i-1}}{(Y_e - Y_s) + 1} \tag{2.1}$$

where:
AGR = Average growth rate;
Y_e = End year;
Y_s = Start year;
P_i = Number of publications on year i;

For the end year Y_e, ScientoPy uses the default global end year configured in the global options or/in ScientoPy command parameters. The start year Y_s is calculated from the end year Y_e, as indicated in the Equation 2.2

$$Y_s = Y_e - (WindowWidth + 1) \tag{2.2}$$

The default $WindowWidth$ is 2 years. Thus, if the end year is 2018, the AGR is the average growth rate between 2017 and 2018.

Average Documents per Year (ADY) The Average Documents per Year (ADY) is an absolute indicator that represents the average number of documents published inside a time frame for a specific topic. The ADY is calculated using the Equation 2.3:

$$ADY = \frac{\sum_{i=Y_s}^{Y_e} P_i}{(Y_e - Y_s) + 1} \tag{2.3}$$

where:
ADY = Average Documents per Year;
Y_e = End year;
Y_s = Start year, calculated as described in Equation 2.2;
P_i = Number of publications on year i;

Percentage of Documents in Last Years (PDLY) Percentage of Documents in Last Years (PDLY) is a relative indicator that represents the percentage of the ADY relative to the total

number of documents for a specific topic. In this way, the PDLY is calculated using the Equation 2.4:

$$PDLY = \frac{\sum_{i=Y_s}^{Y_e} P_i}{(Y_e - Y_s + 1) * TND} * 100\% \tag{2.4}$$

where:
$PDLY$ = Percentage of Documents in Last Years;
Y_e = End year;
Y_s = Start year, calculated as described in Equation 2.2;
P_i = Number of publications on year i;
TND = Total number of documents;

2.1.2 User graphic interface (ScientoPyUI)

We developed a simple graphic user interface (GUI) for the use of ScientoPy called ScientoPyUI (available in `https://github.com/jpruiz84/ScientoPyUI`). This interface allows us to select the preprocess folder and perform a different kind of temporal analysis (see Figure 2.2).

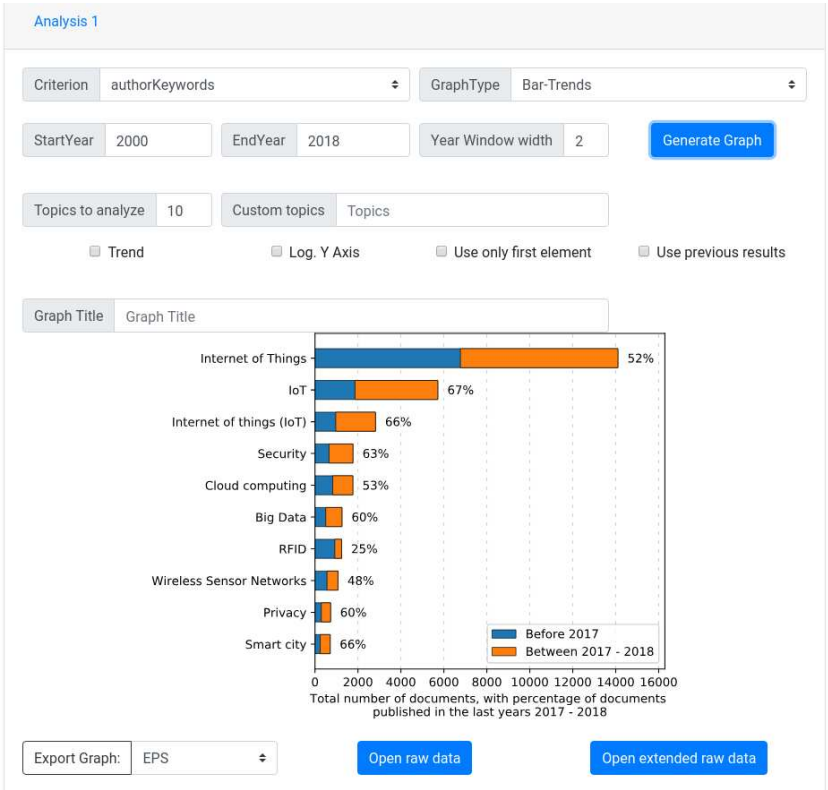


Figure 2.2: ScientoPyUI, graphical user interface analysis window

The main features and capabilities of this GUI are:

- Select the input dataset folder
- Perform the dataset preprocessing with and without the remove duplicate filter
- Select the analysis criterion and graph type
- Define the year range analysis time frame, and the year window width
- Set the topic list length (Topics to analyze)
- Set the custom topics to analyze
- Define customs analyzes options (trend analysis, Y axis in log scale, only first element to analyze, and use previous results)
- Set the graph title
- Export the graph in three different formats (EPS, SVG, and PNG)
- Open the raw and extended raw output data

You can find more information about the different capabilities and the installation instructions of ScientoPyUI by the user manual available in the following link: manual.

2.1.3 Comparative with other scientometric tools

In this section, we discuss 8 different tools (including ScientoPy) designed to make a scientometric quantitative analysis that helps scholars to track innovation progress and to find trending topics. These tools were tested and analyzed from July 1st, 2018 to December 17th, 2018, then, any updates of these tools after the last date are not included. Table 2.7 provides an overview of these tools characteristics. All the tools mentioned here support the datasets from the two main bibliographic databases (WoS and Scopus). Nevertheless, some tools like CiteSpace, Bibliometrix, Networkbench, and Sci2 support more than these two main databases. Notwithstanding, not all tools that support more than one database can merge the information successfully from two or more sources because the source databases do not always use the same fields labeling or fields representation (like the author's names represented different in Scopus and WoS). From these tools, only ScientoPy and Bibliometrix perform the preprocess and merge steps that allow working with the combined information of the databases that they support.

The preprocessing is one of the most critical steps in scientometrics analysis because the goodness of the result will depend on the quality of the data [70]. Duplication removal is one of the main preprocessing steps which allows the quality of the data, primarily if we work with datasets from two different databases. In this analysis, all tools have an implementation for duplication removal except BiblioTools.

Besides, when we use a bibliometric database, we can do search wildcards, like the asterisk (*), in the database's search engine. These wildcards allow us to find not only plural and singular equivalence, even more, help us to find concepts, like "smart*" (smart homes, smart cities, among others). ScientoPy is the only tool in this list that allows us to find topics using the asterisk wildcard. This capability lets us find a singular, plurals, and word concepts inside the downloaded dataset.

Inside the temporal analysis, trend analysis identifies trending topics and their evolution over time. ScientoPy calculates the AGR, finds the topics with the top ones, makes an evolution plot to show the evolution over the time of each trending topic, and compare them according to the absolute growth with the AGR, and the relative growth with the PDLY. CiteSpace uses the burst-detection Kleinberg's algorithm for detecting sharp increases of interest in a specialty. It finds burst terms extracted from titles, abstracts, descriptors, and identifiers of bibliographic records [56]. Others tools, like SciMAT, uses the strategic diagram to plot the topics in a Cartesian plane according to their centrality and density over different periods [54, 61]. As well, Bibliometrix uses the functions KeywordGrotwh and sourceGrowth to calculate yearly published documents for top keywords and source respectively, the thematicMap and thematicEvolution to create a thematic map and evolution analysis based on co-word network analysis and clustering, and the histNetwork to create a historical citation network from a bibliographic data frame [59, 71]. Finally, Network Workbench and Sci2 use the Kleinberg's burst detection algorithm [62] to identify sudden increases in the usage frequency of words over time [72].

The output data could be represented differently by the tools here discussed. The tools specialized in network analysis (CiteSpace, Network Workbench, and Sci2) export the result data into GraphML files. SciMAT and BiblioTools generate Latex reports with graphical and numerical information. Meanwhile, Bibexcel exports tabbed data records to be imported directly to Excel or any spreadsheet tool. Bibliometrix generates R data frames structures with the data obtained after the preprocessing, or analysis routines. Also, it can generate graphical images. ScientoPy can generate different kinds of graphical images that summarize the preprocess, or analysis results. Also, it generates CSV (Comma Separated Values) files that we can easily import into any spreadsheet tool.

The user interface allows us to interact with the different characteristics of each tool. In this field, CiteSpace, SciMAT, Bibexcel Network Workbench, and Sci2 offer a windowed user interface that allows to load the dataset, run the preprocessing steps, and execute the data analysis. In this classification, SciMAT highlights with a wizard menu to perform the analysis steps. In BiblioTools, the user runs some command lines scripts to execute the preprocessing and data analysis. Then the user can navigate through the result plots using a web-based application.

Similarly, Bibliometrix from version 2.0.0 includes a web-interface, namely biblioshiny, which implements the main features of Bibliometrix, including dataset loading, filtering, descriptive analysis (longitudinal analysis, keywords and sources trending), conceptual, intellectual and social structure analysis. Alternatively, for ScientoPy, the users can perform all operations through the command line scripts (preprocessing, and data analysis), or from the ScientoPyUI graphical interface. The command-line option allows the user to generate a single batch script that performs all the operations needed for a particular analysis.

Table 2.7: Scientometrics tools

Tool	Supported databases	Duplication removal	Search with wild-card	Trend analysis	Output	User interface	Reference
ScientoPy	WoS and Scopus	Yes	Yes	AGR, evolution plot	Graphical images, and TSV files	Command line / windowed JavaScript application	
CiteSpace	WoS, Scopus, CSCD, CSSCI, CNKI, or PubMed	Yes	No	burst-detection	GraphML, Pajek, HTML, CSV report	Windowed Java application	[56]
SciMAT	WoS or Scopus	Yes	No	Strategic diagram	Graphical images, and HTML or Latex report.	Windowed Java application	[54]
Bibexcel	WoS or Scopus	Yes	No	No	Tabbed data records	Windowed application	[55]
Bibliometrix	(WoS and Scopus) or Cochrane Library or PubMed	Yes	No	KeywordGrowth, sourceGrowth, thematicMap, thematicEvolution, and histNetwork‘	R data frames, and graphical images	biblioshiny web-interface	[59]
Network Workbench	Scholarly Database (SDB), Bibtex, WoS, Scopus or Google Scholar	Yes		Bursting words	Graphical images, GraphML, XGMML and Pajek files	Windowed application	[72]
BiblioTools	WoS or Scopus	No	No	No	Web based interface and Latex report.	Command line / web based	[73]
Sci2	WoS, Scopus, Endnote, or BibteX	Yes	No	Burst detection	GraphML, NWB, Pajek, XGMML, and CSV	Windowed application	[74]

2.2 Internet of things

Internet of Things (IoT) connects billions of devices to the Internet and has gained tremendous popularity in the past decade as a diverse and pioneering technology. In general, IoT devices combine sensing, computation, and communication techniques to deliver remote data collection and system control. Today, these "things" range from everyday consumer electronics to specialized industrial systems [75], such as fitness-tracking wristwatches [76], transport logistics [77], and smart cars [78] to manufacturing [79] and smart grids [80]. Contingent on implementation, an IoT device may be used for real-time alerts, data archiving, trend analysis, and forecasting by leveraging related technologies such as cloud services [81]. Furthermore, the technology has proven useful for small- and large-scale networks, generating a vast portfolio of enabling hardware and software at various complexities [82, 83]. IoT technology has led to solutions in use-cases ranging from smart appliances, utilities, biomedical, industrial, data center management, agriculture, body area networks (BANs), surveillance, and more.

Proliferation of IoT research has contributed to increased availability, affordability, responsiveness, diversity, miniaturization, mobility, and more. Recent studies have demonstrated that IoT, cloud computing, and mobile solutions are among the top technologies that will shape our future in the next 3–5 years [81]. Not surprisingly, connectivity and intelligence are becoming a contributing factor to many designs fueling advanced development. Therefore, the number of new designs and publications categorized under IoT continues to grow exponentially.

Evolution of IoT has spearheaded many research fields such as wireless sensor networks (WSNs), Big Data, and cloud computing. Wireless Sensor Networks (WSN) comprise: sensor nodes, specialized firmware [84], relay devices, and data sinks called a gateway. In addition to facilitating data archiving and local processing, the gateway also acts as a hub that connects to the worldwide web for cloud storage and services using a WiFi or cellular network.The computational complexity of analysis and functional use of the data towards trend and forecasting has grown rapidly, such as in the data center management use-cases [85]. The radio frequency (RF) communication protocols and the interaction between these sensor entities continue to place stringent hardware requirements. Implementations using one software stack over another could achieve better range, quality-of-service (QoS), and spectral efficiency, at the expense, however, of additional processing, storage, power, and form-factor [83]. Additionally, the connectivity and archiving with WSN results in a large volume of samples that create a "big data" challenge.

While IoT is not a new paradigm, it is gaining traction in recent years around the world and yielding extensive research from diverse perspectives. As a result, IoT and similar technologies are progressively challenging topics to review. Starting in 2010, Atzori et al. made a survey about IoT enabling technologies and applications [86]. Then, in 2013, Gubbi et al. defined a cloud center vision for worldwide implementation of IoT, describing the key enabling technologies, applications domains and future directions [1]. In 2014, Borgia presented an extended review about IoT key features, driving technologies and protocols, applications, challenges, IoT initiatives, and research directions [87]. Next, in 2015, Yan et al. developed a co-word analysis, generating seven clusters that represented the intellectual structure of IoT, which were analyzed by a co-occurrence matrix [88]. The following year, in 2016, Mishra et al. composed a bibliometric study about the future vision, applications, and challenges of Internet of Things [89]. In that review, Mishra et al. identified the top contributing authors, key research topics, most influential works, and emerging research clusters, limited only to future vision and applications of IoT, from a

sample of 1556 papers from the Scopus database.

As noted above, when conducting a review of IoT publications in recent years, the outcome may vary depending on methodology and time spent browsing through search results. At a minimum, only publications of reputable categories from credible databases should be considered for the review process. For example, conference papers, journal articles, proceedings papers, and reviews are widely accepted as reliable information sources in the industry and academia. Additionally, the manual labor of searching thousands of bibliographic data can be reduced by scripting to facilitate the filtering and comparison activities. This allows the reviewer additional time to investigate supplementary metrics in order to render stronger and methodological conclusions.

2.2.1 Bibliometric dataset

This scientometrics analysis used two bibliographic databases: Clarivate Web of Science (WoS), and Scopus. For the span of 1 January 2002 to 31 December 2018. The search string for this analysis was "Internet of Things". This string was applied to the topic search in WoS and Scopus, which includes title, abstract, authors' keywords, and KeyWords Plus® (for WoS). With this search criteria, the data set was extracted within a day on 6 July 2017. Table 2.8 describes the number and type of documents found in the two databases totaling 27,120 documents.

Table 2.8: Type of documents found with the search string "Internet of Things" found in Clarivate Web of Science (WoS) and Scopus within one day on 6 July 2017.

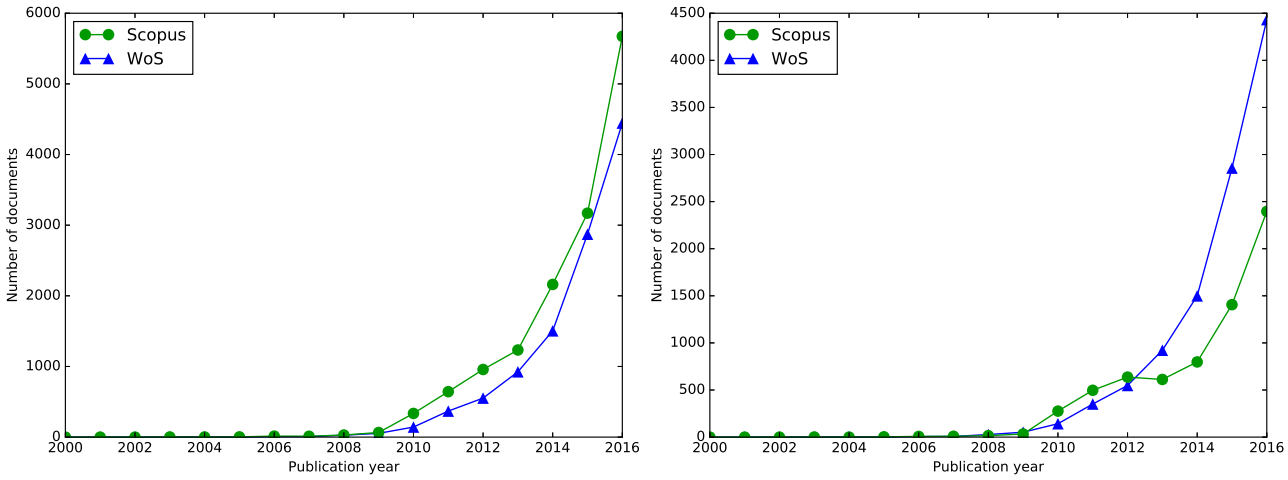
Source	Article	Conference Paper	Proceedings Paper	Review	Duplicated Removed
WoS	3112	0	8215	130	55
Scopus	5283	10,068	0	312	8030

2.2.2 General IoT Publications Growth

The yearly growth of IoT related documents were observed as in Figure 2.3a, revealing an exponential growth in both databases (WoS and Scopus), without removing the duplicated documents. Figure 2.3b shows the similar growth after removing the duplicated documents.

The first mention of the "Internet of Things" was an article published in March 2002 reported by WoS. Published by Forbes, Schoenberger, and Upbin, this article described how the IoT could be a standardized way to help the computers understand the world [90]. In 2003, Scopus reported a paper from the Institute of Electrical and Electronics Engineers (IEEE) International Conference on Systems, Man and Cybernetic, in which Qui and Zhang showed the design of enterprise web servers supporting instant data retrieval for a product labeled with an Radio-frequency identification (RFID) based smart tag [91]. Scopus reported a second conference paper in 2003 for the 36th Annual Hawaii International Conference on System Sciences, Traversat et al. on the stated the JXTA (abbreviation of Juxtapose) protocols as a foundation of the upcoming Web of Things [92].

In 2004, WoS and Scopus reported the same two articles: "The Internet of Things" by Gershenfeld et al. [93], and "The Supply Chain" by Luckett [94]. From 2005 to 2016, Scopus



(a) (b)

Figure 2.3: Documents per year published (WoS and Scopus) with the search string "Internet of Things" (IoT) for the period 2000 to 2016. (**a**) before the duplicates-removal filter; (**b**) after duplicates-removal filter.

reported about 30% more publications than WoS. Nevertheless, for this research, WoS documents were given more priority over Scopus documents during the duplicates-removal process because WoS fields were more complete than Scopus, such as cited references with Digital Object Identifier (DOI) number and subject category. For this reason, Figure 2.3b shows more documents from WoS than Scopus from 2013 onwards.

2.2.3 Country and Author Research Analysis

In this section, analysis was focused on authors and their corresponding country. Below is a graph of the percentage of publications related to IoT each year for the seven countries with the highest occurrence in the data set. A table of the most occurring 50 countries is also provided. Another graph presents the top five authors per year, alongside tables detailing the top 20 authors and 10 most cited author documents for articles, conferences and reviews.

Country Analysis

A list of the countries with the most associated publications was generated. Figure 2.4 shows the top seven countries, along with the percentage of documents published per year. In 2002, one article was published on Forbes by Schoenberger; unfortunately, the database does not associate any author address for this document and the sample had to be removed from this data set according to methodology. In 2003, two conference papers were published by United States authors [91, 92]. In 2004, there was one review publication in the United States [93] and one article in the United Kingdom [94].

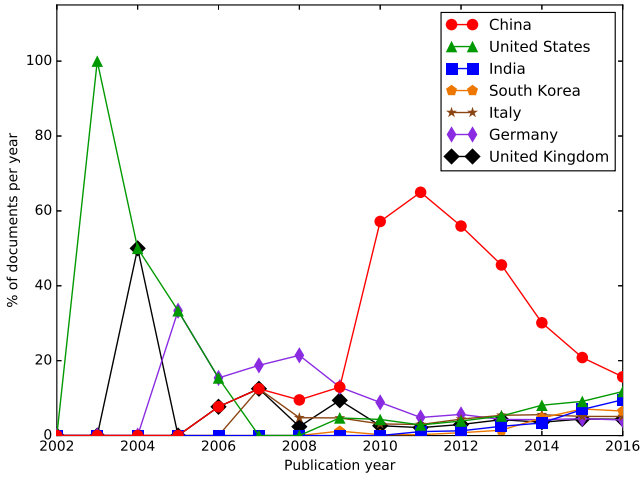


Figure 2.4: Internet of Things percentage of documents published per year by the top 7 first author's corresponding address country for the period 2002 to 2016.

Germany [95] and Malaysia [96] first appear in 2005, joined by the United States [97]. These three conference papers demonstrated how the RFID can boost Internet of Things for manufacturing, packing, tracking, and automobile logistics. In 2006, the total publications grew from 3 to 12, with more countries participating, such as France [98, 99], Switzerland [100, 101], and Japan [102]. From 2006 to 2009, Germany led the number of publications with 2, 3, 9, and 11, respectively. During that period, the German author Broll led the citations count with a proposed framework for integrating web services and mobile interaction with physical objects [103].

China drastically increased from 11 to 239 publications from 2009 to 2010, continuing to contribute more than half of the globally published documents between 2010 to 2013. Most of that growth resulted from China's Twelfth 5 Year Plan (2011–2015), which included the development of the Internet of Things [104]. The conference paper "IOT Gateway: Bridging Wireless Sensor Networks into Internet of Things" by Zhu was the most cited IoT paper during this period for China, as it explained how an IoT Gateway could make a bridge between wireless sensors networks and traditional communications networks to the Internet [105].

From 2014 to 2016, China maintained the highest rank, contributing 20% of the globally published documents, as well as a peak in 2016 and h-index of 47. In 2014, the United States was second to China with 187 publications and h-index of 42. India's contributions grew at a rate of 153%, 103%, 286%, and 120%, in 2013 to 2016, respectively, moving from the 8th to 3rd position in 2013 and 2016, respectively. The Indian daily "The Economic Times" forecasted the country is expected to see a rapid 31-fold growth of IoT devices to reach 1.9 billion by 2020 [106].

Expanding the results from Figure 2.4, Table 2.9 shows the top 50 countries of the primary author with the average percentage growth and the h-index of each country from the last three years (2014 to 2016). Of the top 10 countries, South Korea represents the maximum average growth with 206%, where the mobile carrier SK Telecom (Seoul, South Korea) launched the first commercial low-cost Internet of Things (IoT) network in 2016 [107]. However, this growth is not reflected yet (next year) in the available literature and thus the data set has an h-index of 16, only half of its successor in this list, Italy. In the same way, this list includes the top growing countries with low h-index but anticipated to be higher next year: Indonesia, Turkey, Russian Federation, and Pakistan.

Table 2.9: Internet of Things top 50 countries of first author's corresponding address. Country number position (N.), total number of publications (Total), average percentage growth from the last 3 years (2014 to 2016), and h-index (h-ind.) from 2006 to 2016.

N.	Country	Total	Average Growth	h-Ind.
1	China	4822	16%	47
2	United States	1561	116%	42
3	India	1089	169%	15
4	South Korea	894	206%	16
5	Italy	874	61%	32
6	Germany	811	64%	24
7	United King.	711	71%	25
8	France	543	126%	21
9	Spain	463	42%	23
10	Japan	449	166%	11
11	Taiwan	438	68%	16
12	Brazil	272	90%	9
13	Finland	266	50%	20
14	Canada	259	104%	15
15	Australia	249	59%	22
16	Sweden	216	68%	17
17	Switzerland	193	31%	19
18	Portugal	191	45%	13
19	Greece	180	46%	14
20	Romania	169	72%	9
21	Belgium	164	87%	11
22	Austria	146	113%	12
23	Malaysia	137	71%	9
24	Russian Fed.	134	271%	8
25	Ireland	126	116%	9
26	Netherlands	109	122%	12
27	Singapore	109	112%	8
28	Poland	104	77%	6
29	Czech Rep.	101	153%	5
30	Turkey	92	319%	5
31	Pakistan	82	210%	7
32	Saudi Arabia	80	122%	7
33	Norway	72	119%	11
34	UAE	71	180%	6
35	South Africa	60	162%	9
36	Denmark	59	39%	11
37	Tunisia	55	163%	6
38	Serbia	53	−1%	6
39	Croatia	51	159%	6
40	Hungary	51	24%	6
41	Indonesia	51	410%	3
42	Egypt	49	159%	4
43	Morocco	47	163%	4
44	Iran	42	94%	5
45	Colombia	39	146%	3
46	Algeria	38	113%	5
47	Jordan	38	108%	5
48	New Zealand	38	86%	6
49	Mexico	36	172%	5
50	Thailand	32	107%	4

The International Data Corporation (IDC) predicts that, by 2019, 20% of local and regional governments in Indonesia will use the Internet of Things to turn infrastructure such as roads, street lights, and traffic signals into assets instead of liabilities [108]. In addition, the Dutch IoT start-up, Xeelas (Arnhem, Netherlands), and Turkish group, Sade (Ankara, Turkey), partnered to

build Turkey's largest LoRaWAN (LoRa, Long Range Wide-area network network) in Istanbul to enable business, local governments, and conservation groups to collect and analyze from connected devices [109]. In Russia, the Internet of Things market is expected to reach USD 74 Billion by 2023, where the Russian government's Internet start-up fund (FRII) has joined forces with tech giants GS Group (Saint-Petersburg, Russia) and mobile operators to launch a national Internet of Things (IoT) consortium [110]. In Pakistan, by January 2017, 17 Internet of Things start-ups were launched, on their own or incubated, at Plan9 (Lahore, Pakistan), NEST i/o (Karachi, Pakistan), and i2i (Islamabad, Pakistan) [111].

Author Analysis

The data set analyzed here includes 31,422 authors of the 19,035 documents related to Internet of Things. In addition, 592 of these authors have 10 or more publications in WoS or Scopus. Figure 2.5 shows the top five authors with the most published documents per year. Y. Zhang was positioned first with 130 published documents related to IoT and RFID, security, electric vehicle, artificial immune system, smart grid, and cloud computing. In 31 documents, Y. Zhang appeared as a first author. His most cited document is the article titled "Toward Cloud-Based Vehicular Networks with Efficient Resource Management" [112] with 96 citations.

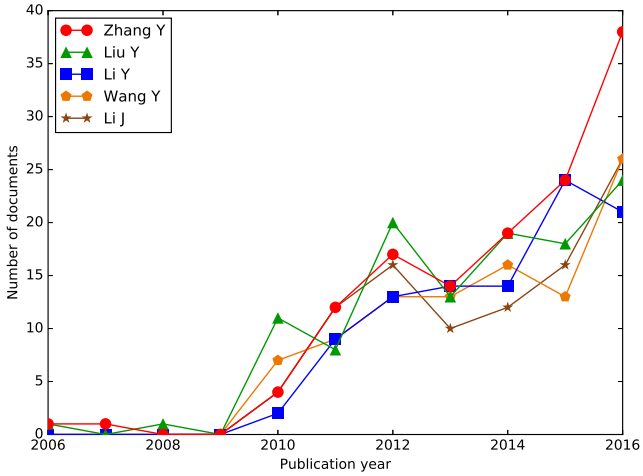


Figure 2.5: IoT top 5 authors
Internet of Things top 5 authors with most documents published per year, for the period 2006 to 2016.

Y. Liu is positioned second with 115 documents, of which 36 list him as the primary author. His publications are more focused on hardware such as Raspberry Pi, test bed, optical communications, ZigBee, and RFID. The article titled "IOT gateway: Bridging wireless sensor networks into Internet of Things" is his most cited document with 134 citations [105]. Y. Liu shares the authorship in four publications with the first author in this list, Y. Zhang.

Y. Li is the third in this list with 97 publications, with 37 as the primary author. His focus was on RFID, big data, and databases. "Towards a theoretical framework of strategic decision, supporting capability and information sharing under the context of Internet of Things" [113] is his most cited publication with 39 citations. With the same number of publications, 97 and 39

as the primary author, Y. Wang is next in this list. His research is related to RFID, smart gird, security, logistics, and big data. His most cited document is [114] with 16 citations. Lastly, fifth on this list is J. Li with 96 publications with 33 as the primary author. His papers related to RFID, ZigBee, and standardized breeding, with his proceedings paper in [115] being his most cited paper with 97 citations in this set.

Table 2.10 shows the top 20 authors with the most published number of documents, along with the author's h-index in IoT, most cited document, and top research topics. Nevertheless, the two-top h-index authors in this case are not in the top 20 number of documents. L.D. Xu is the author with the highest h-index of 21 and 33 publications. Similarly, L. Atzori has second place in h-index of 14 and 41 documents.

Table 2.10: Internet of Things, top 20 authors with most publications, total number of documents, h-index, most cited document, and top related research topics for the period 2006 to 2016.

N.	Author	Total Documents	h-Index	Most Cited Document	Top Author Topics
1	Zhang, Y.	130	12	[112]	RFID, security, Electric vehicle
2	Liu, Y.	115	11	[105]	RFID, name service, ZigBee
3	Li, Y.	97	9	[113]	RFID, big data, database
4	Wang, Y.	97	5	[114]	RFID, smart grid, secirity
5	Li, J.	96	9	[115]	RFID, ZigBee, standarized breeding
6	Zhang, J.	82	6	[116]	RFID, WSN, monitoring system
7	Wang, J.	80	8	[117]	RFID, 5G, sampling
8	Zhang, L.	79	13	[118]	Cloud computing, cloud manufacturing, ZigBee
9	Wang, X.	78	6	[119]	RFID, ZigBee, service selection
10	Chen, Y.	72	8	[120]	RFID, WSN, ZigBee
11	Jara, A.J.	72	13	[121]	6LoWPAN, smart cities, big data
12	Zhang, X.	72	6	[122]	Logistics, RFID, WSN
13	Li, H.	71	7	[123]	RFID, authentication, security
14	Wang, H.	70	9	[124]	RFID, monitoring, cloud computing
15	Li, X.	67	8	[125]	RFID, recommendation, smart grid
16	Liu, J.	65	10	[126]	Cloud computing, RFID, security
17	Kim, J.	62	7	[127]	WSN, video streaming, HEVC
18	Wang, Z.	60	8	[128]	RFID, GPRS, EPC network
19	Liu, X.	59	9	[129]	Cloud computing, RFID, Landsenses ecology
20	Kim, D.	58	7	[130]	EPCIS, 6LoWPAN, security

Table 2.11 shows the most cited papers for three document types (articles, conference/proceedings and reviews). Atzori et al. surveys IoT vision and enabling technologies [86]. Second in articles, Gubbi et al. describe a cloud-centered vision for the worldwide implementation of IoT [1]. Miorandi et al.'s article surveys on technologies, applications and research challenges for IoT [131]. For conferences and proceedings, Bonomi et al. describe the Fog computing characteristics and its role in IoT [132]. Tao et al. propose cloud computing, Internet of Things, virtualization, and service-oriented combination technologies with advanced manufacturing models and enterprise information technologies to generate a new manufacturing model, called cloud

manufacturing (CMfg) [133]. Tan and Wang show a skeleton of the Internet of Things with an application model that can apply to automatic facilities management in the smart campus [134].

Finally, on the reviews side, Gershenfeld et al. present a review about the Internet-0 (Internet-Zero) protocol, whose approach for the reduced complexity of the IP stack extends the notion of internetworking to interdevice [93]. Meng and Ci mention that the data type and amount is growing at a high speed due to emerging services such as cloud computing, IoT, and social media. Thus, they review the concept of big data and describe a new era for data handling [135]. Lastly, Aziz et al. surveys the topology control techniques for extending the lifetime of battery to power WSNs for the Internet of Things battery-powered devices [136].

Table 2.11: Internet of Things top 10 documents with most citations, divided by document type, including position number (N.), first author, document reference, times cited, publication year, and first author corresponding address for the period 2002 to 2016.

N.	First Author	Document Reference	Times Cited	Publication Year	Country
Articles documents					
1	Atzori L	[86]	3239	2010	Italy
2	Gubbi J	[1]	1369	2013	Australia
3	Miorandi D	[131]	721	2012	Italy
4	Kortuem G	[137]	506	2010	United Kingdom
5	Ganti RK	[138]	494	2011	United States
6	Bobadilla J	[139]	482	2013	Spain
7	Li B-H	[118]	471	2010	China
8	Perera C	[140]	454	2014	Australia
9	Zanella A	[141]	404	2014	Italy
10	Chen M	[142]	370	2014	China
Conference and proceedings documents					
1	Bonomi F	[132]	508	2012	United States
2	Tao F	[133]	228	2011	China
3	Tan L	[134]	169	2010	China
4	Spiess P	[143]	156	2009	Not specified
5	Mainetti L	[144]	142	2011	Italy
6	Zhu Q	[105]	134	2010	China
7	Dohr A	[145]	132	2010	Austria
8	Kovatsch M	[146]	112	2011	Switzerland
9	Khan R	[147]	101	2012	Italy
10	Su KH	[115]	97	2011	China
Review documents					
1	Gershenfeld N	[93]	271	2004	United States
2	Meng X	[135]	172	2013	China
3	Aziz AA	[136]	139	2013	Malaysia
4	Domingo MC	[148]	138	2012	Spain
5	Borgia E	[87]	132	2014	Italy
6	Hancke GP	[149]	101	2013	South Africa
7	Wang ZL	[150]	98	2010	United States
8	Wang SH	[151]	83	2015	United States
9	Keoh SL	[152]	69	2014	Singapore
10	Malhotra A	[153]	64	2013	United States

2.2.4 Research Topics

IoT has a broad spectrum of research fields such as applications, smart objects, communications protocols, software processing, devices hardware, and operating systems. On the data set analyzed here, most of the authors include their research topic in the document keywords. In this section, author keywords were analyzed to find the trends in the different research topics. For Scopus, the regular authors' keywords were used, and similarly for WoS. KeyWords Plus from WoS were discharged because they are index terms created automatically from significant, frequently occurring words in the titles of an article's cited references, and they are less comprehensive in representing an article's content [154]. The top 1000 keywords were extracted, manually classified in the different research field, and grouped by plural-singular similarity and/or abbreviations. For instance, the keywords WSN, wireless sensor network, and wireless sensor networks were grouped into the WSN keyword. The following subsections describe the trend of the research topics in different fields, based on the top authors' keywords publications per year. Figure 2.6 shows the general top 10 authors' keywords.

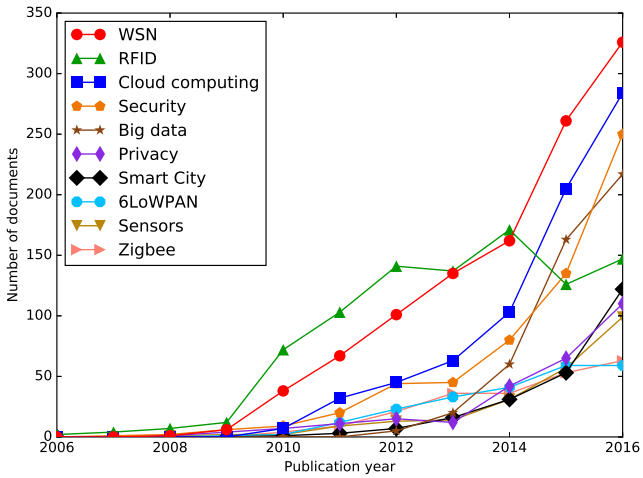
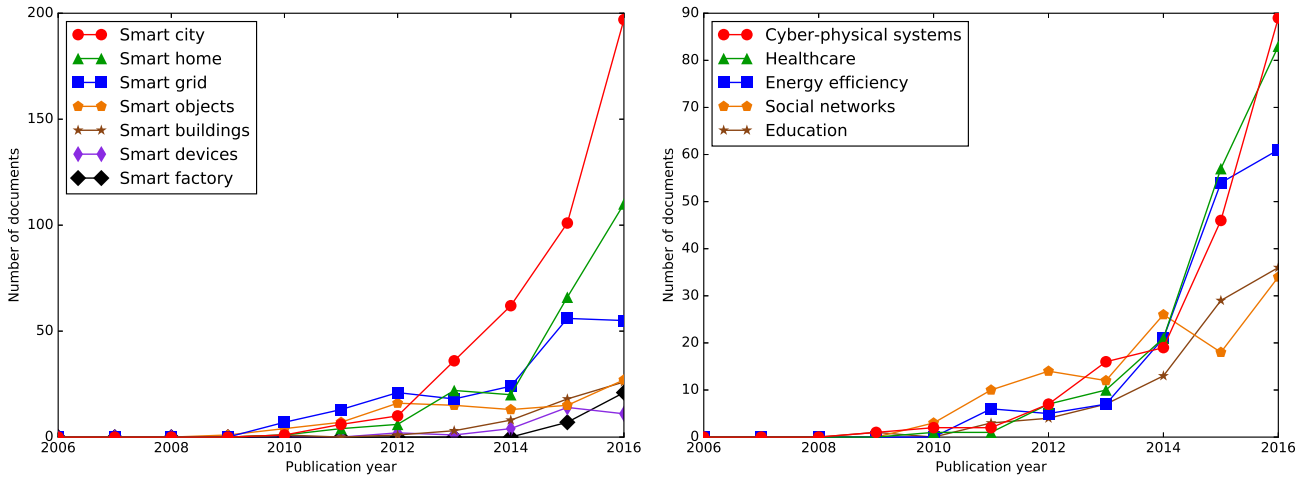


Figure 2.6: IoT top authors' keywords
Internet of Things top authors' keywords documents published per year, excluding the keywords: Internet of Things, IoT, Internet of Things (IoT), and The Internet of Things, for the period 2006 to 2016.

Applications

There are several application fields related to IoT research and development. In this section, the authors' keywords were analyzed to find the top specified applications. Figure 2.7 shows the trend of these applications in documents per year. Furthermore, Figure 2.7a presents the applications that start with the word "smart", and Figure 2.7b those that do not.



(a) (b)

Figure 2.7: Internet of Things top applications based authors' keywords in documents per year, for the period 2006 to 2016. (**a**) applications that start with "smart" (**b**) applications that do not start with "smart".

In the data set, 1052 documents were found for applications that start with "smart". Smart city is the top one in this list, with 413 documents, and a sigmoid growth in exponential phase, 95% more publications in 2016 vs. 2015. A.J. Jara has the most number of documents in this field with 12 publications. His most cited document [155] refers to Smart and Connected Communities as a concept that is evolving from Smart cities. The leading country in this application is Italy with 50 publications, and the most important correlated topics are Big data [156–158], Cloud computing [159,160], and Smart grid [161,162]. Similarly, Smart home has a linear growth, with 230 documents, and 111 in the last year, with China as the leading country. The most important related topics for Smart home are security [163–165], ZigBee [166–168], and activity recognition [169–171].

In contrast, smart grid is a topic that has not demonstrated continuous growth. In 2012–2013, the documents published per year decreased from 21 to 13, and in 2015–2016 from 56 to 55. Nevertheless, an overall 194 documents were registered on this topic, with China as the leading country. The term smart grid refers to "a next generation power grid that uses two-way flows of electricity and information to create a widely distributed automated energy delivery network" [172]. Within IoT, the research on smart grids are related to security [173–175], cloud computing [176,177], and privacy [175,178,179].

According to Dumitrache, "Cyber-Physical Systems (CPS)s are physical, biological and engineered systems whose operations are monitored, coordinated, controlled and integrated by a computing and communication core" [180]. Publications of this topic related to IoT have a sigmoid growth in exponential phase, with 182 publications in 2016, noting United States as the leading country with 34 documents. The most important related topics are: Industry 4.0 [181–184], big data [185–187], and security [188–190]. Next, Healthcare and E-Health related to IoT exhibited a sigmoid growth in a transitional phase, with a total of 180 documents, and India as the leading country with 20 publications. Different IoT technologies are applied in this area such as sensors [191], RFID [192–195], 6LoWPAN [196,197], and wearables [198,199]. The third most growth topic was energy efficiency with 154 documents, and China and Italy

as leading countries with 18 and 17 publications, respectively. Energy efficiency as an application for IoT is related in this data set with the following topics: smart buildings [200–202], energy harvesting [203–205], and RFID [206, 207]. Social networks (or Social media) is another application for IoT, with 117 documents, and Italy as the leading country with 23 publications. Among the top related topics in this field are trust management [208–210] and recommendation systems [211, 212]. Education, Learning, E-Learning, and mobile learning is the fifth top application in this list, with 93 publications and the United Kingdom as the leading country with 12 documents. The most popular related topics with education are: augmented reality [213–215], context aware [216–218], and near field radio technologies such as RFID [219–221] and Near Field Communication (NFC) [222, 223].

Smart city

Smart city is a core component for this research work with applications related to Intelligent Transport Systems (ITS), smart mobility, and smart transportation. With the purpose to find the relationship between these applications, a co-occurrence map was generated in VOSViewer (see Figure 2.8). Here we find a strong relationship between IoT and smart city. Then, smart city is correlated with smart transportation [224], ITS [225], and smart mobility [226, 227]. Similarly, we found here that due to the huge quantity of data generated by the transportation applications, we found a strong relationship between them and big data [228–231]. Finally, we found that the transportation application here are related also with simulation analysis [232–234].

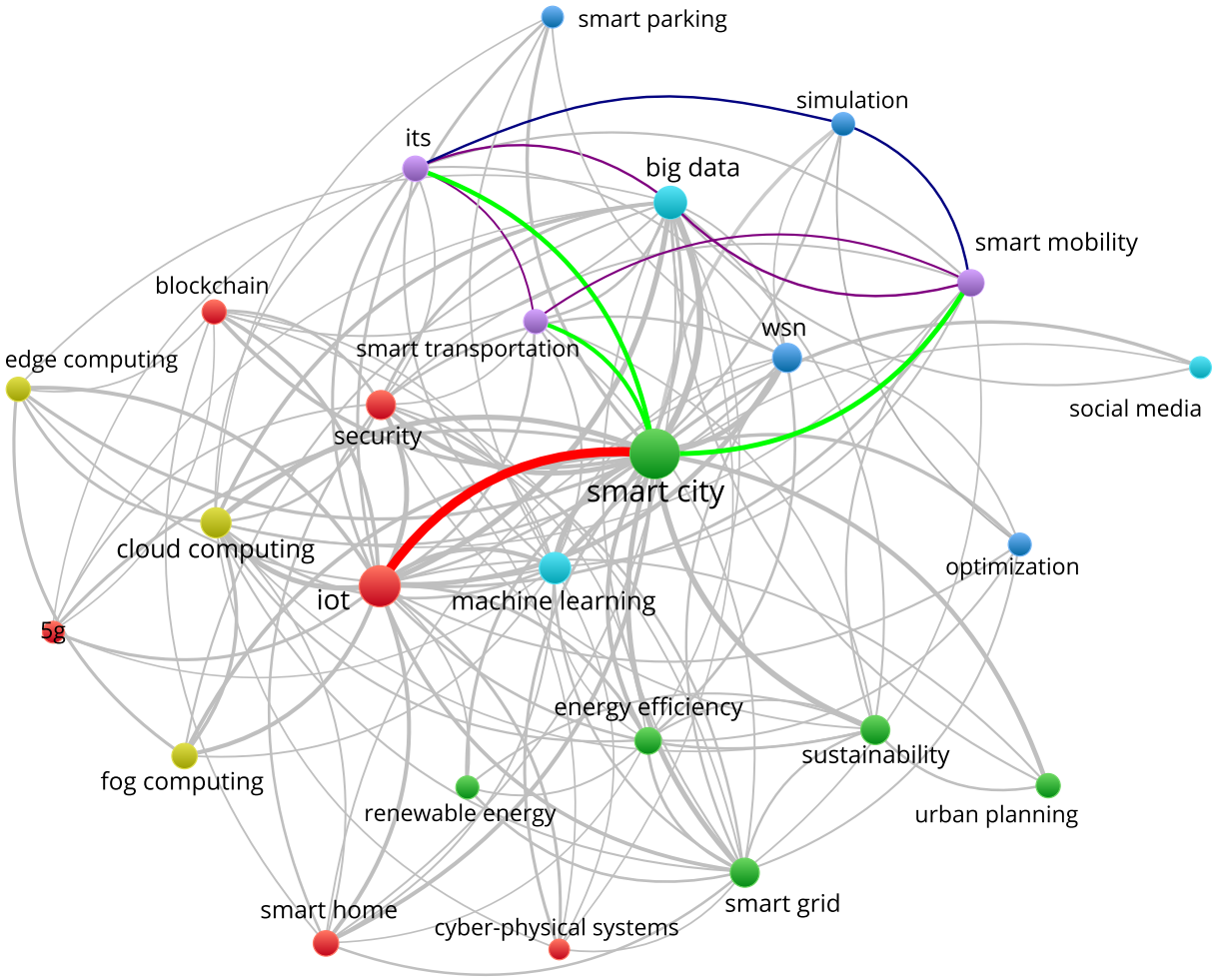


Figure 2.8: Internet of Things and Smart City applications correlation.

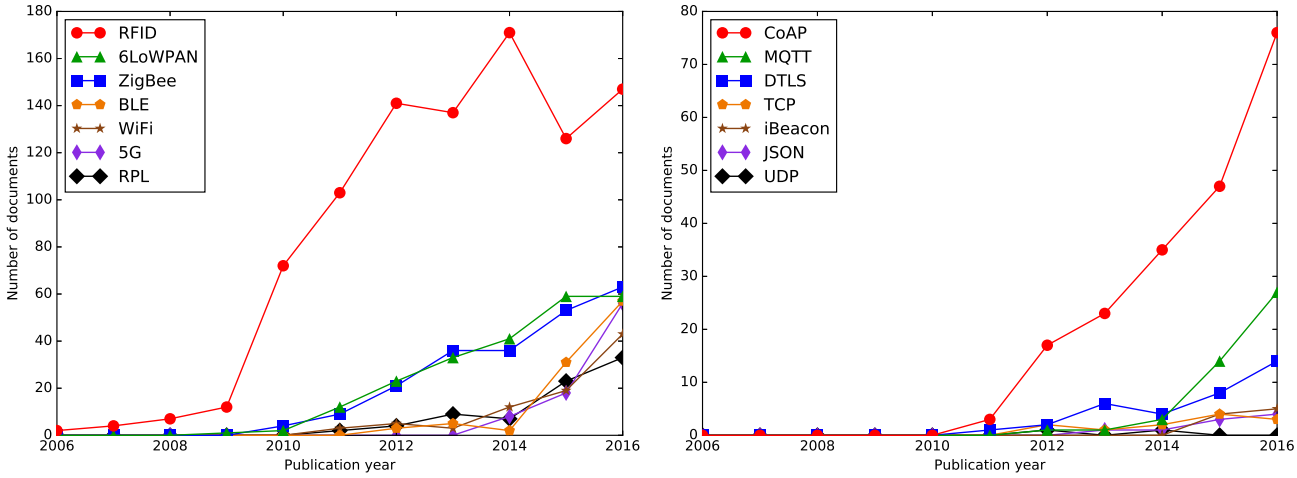
Communication protocols

Regarding telecommunications systems, the Open Systems Interconnection model (OSI model) describes the communications process in seven layers which are divided into media layers (Physical,Data, and Network) and host layers (Transport, Session, Presentation, and Application) [235]. In this review on IoT, the most used communication protocols are divided into these two layers (see Table 2.12). Figure 2.9 shows the yearly trend of the different communications protocols for media layers in Figure 2.9a and host layers in Figure 2.9a.

Table 2.12: Internet of Things Open Systems Interconnection model (OSI model) communication protocols.

	Layer	IoT Communication Protocols
Host layers	7. Application 6. Presentation 5. Session	CoAP, MQTT, JSON, iBeacon
	4. Transport	TCP, UDP, DTLS
Media layers	3. Network	IPv6, 6LowPAN, ZigBee, BLE, RPL
	2. Data link 1. Physical	RFID, 802.15.4, WiFi, BLE, 5G

Abbreviations definition: Constrained Application Protocol (CoAP), Message Queue Telemetry Transport (MQTT), JavaScript Object Notation (JSON), Transmission Control Protocol (TCP),User Datagram Protocol (UDP), Datagram Transport Layer Security (DTLS), Internet Protocol version 6 (IPv6), IPv6 over Low-Power Wireless Personal Area Networks (6LoWPAN), Bluetooth Low Energy (BLE), Routing Protocol for Low power and Lossy Networks (RPL), Radio-frequency identification (RFID).



(a) (b)

Figure 2.9: Internet of Things media and host layers communication protocols based on authors' keywords in documents per year, for the 2006 to 2016 period. (**a**) media layers' communications protocols (**b**) host layers' communication protocols.

RFID is the top used author's keyword in the analyzed data set and the most used media layer communication protocol in the authors' research. On IoT 923 publications are related to RFID, where security authentication [236–238], wireless sensors networks [239,240], privacy [241, 242], and electronic product code (ECP) [243, 244] were major applications. Next, 6LoWPAN appears in 230 publications, with documents related to upper layer protocols such as Constrained Application Protocol (CoAP) [245, 246], Routing Protocol for Low power and Lossy Networks (RPL) [247, 248], and operating systems like Contiki [249, 250], and Android [251, 252]. With

similar growth, ZigBee follows with 222 documents, and research integrates this protocol with solutions such as RFID [253–255], or applications like smart home [167, 256, 257], and health care [258–260].

Bluetooth Low Energy (BLE) has experienced a rapid growth in the last three years, near 100% from 2015 to 2016. A total of 98 documents on IoT are related to BLE, with one of the most cited articles by Gomez et al. at 176 citations. In this article, the authors describe the main features and potential applications for BLE technology [261]. This data set shows BLE related applications such as home automation [262–264] and indoor location [265–267] and health care [268–270]. WiFi is the other network protocol used for IoT research, with a total of 85 publications, and applications related to: home automation [271, 272], indoor localization [273]. Nevertheless, with this wireless technology, some authors have focused on how the 2.4 GHz spectrum could be efficiently used with other IoT network protocols [274–280]. Similarly, 5th generation mobile networks (5G) appear in IoT with 82 publications, much more than 4G and LTE, with 54 documents both combined. The most cited paper is a suvery on 5G architecture and emerging technologies written by Gupta et al. [281] with 109 citations. Network Function Visualization (NFV) and Software Defined Networking (SDN) [282–284] were the top related technologies, which offer different architectural options to address IoT needs for 5G. Finally, RPL is discussed as an IPv6 Routing Protocol for Low-Power and Lossy Networks as a mechanism for multipoint-to-point and point-to-multipoint traffic for these kinds of networks [285]. This protocol has 78 documents with publications related to the Contiki OS and its simulator tool Cooja for WSN [286, 287], and mesh networks [288–290].

At the host layer, communication protocols publications are led by the Constrained Application Protocol (CoAP), which is a specialized web transfer protocol for use with constrained nodes and constrained networks [291]. A total of 201 publications were found in this area, with some of these publications related to: 6LoWPAN [246, 248, 292], and Datagram Transport Layer Security (DTLS) [293, 294]. Second, the Message Queue Telemetry Transport (MQTT) shows up with 46 documents. This is a lightweight, and open client-server publish/subscribe messaging transport protocol [295]. Next, Datagram Transport Layer Security (DTLS) protocol follows this list with 35 publications. This DTLS provides communications privacy for datagram protocols based on the stream-oriented Transport Layer Security (TLS) [296]. This protocol helps to enhance the security of others' higher layers protocols like CoAP [297, 298]. Finally, iBeacon is the fifth on this list with nine documents. This is a protocol designed by Apple (Cupertino, CA, United States) to describe its own implementation of BLE Beacon, which emits a signal that can be detected by any BLE enabled device within a close range [299]. Most of the applications for this protocol include indoor localization [122, 300].

Software Processing Techniques

The proliferation of IoT has significantly increased the data collection and the strain it places on faster data analytics. Several software processing techniques have been researched, developed, and published. In these published documents, the various software processing techniques used were specified in the authors' keywords. Figure 2.10 shows the top authors' keywords for these processing techniques. Machine learning is the most popular research technique for data processing with 100 publications. This technique is used for data prediction [301, 302], activity recognition [303, 304], and data classification [305, 306]. Next, data mining appears with 89 documents, with distributed data mining [307], and applications such as event detection [308, 309]

as sub-techniques.

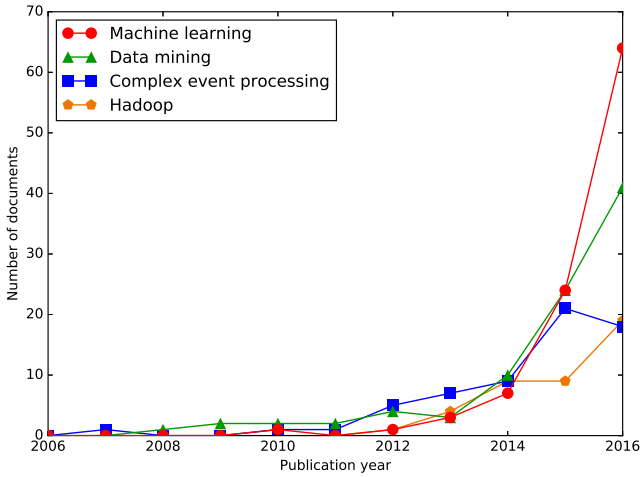
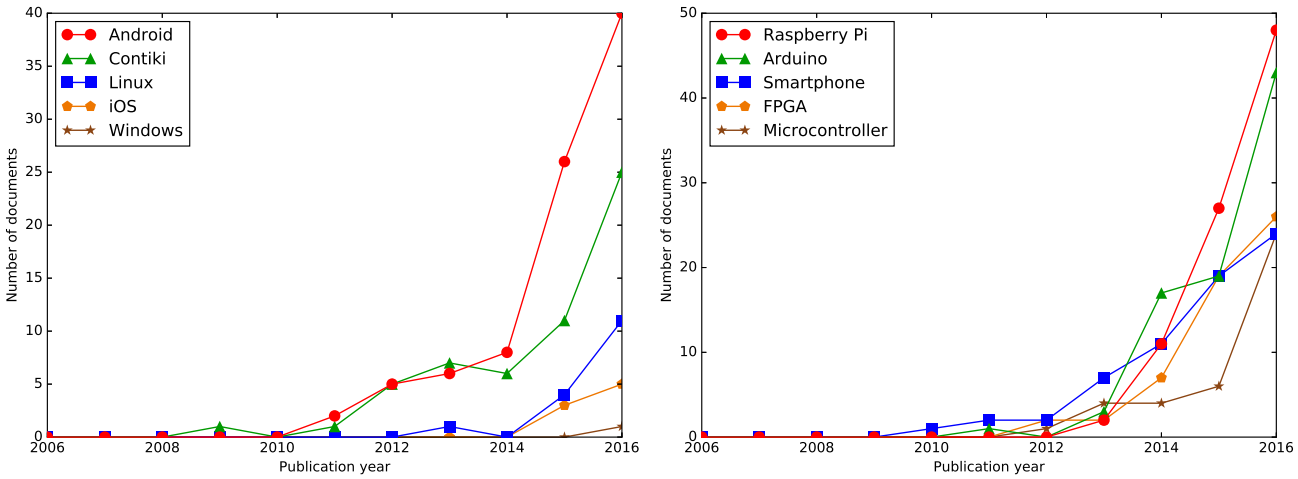


Figure 2.10: IoT software processing techniques
Internet of Things software processing techniques based on authors' keywords in documents per year, for the period 2006 to 2016.

Complex event processing is a method of tracking and analyzing streams of data surrounding events or anomalies and basing a conclusion from them [310]. It was found that 63 documents are related to this processing technique with applications such as supply chain [311–313] and health care [314,315]. Apache Hadoop (or Hadoop) is a software framework used for distributed storage and big data processing using the MapReduce programming model [316], appearing with 42 documents and applications including smart cities [317–319], and Social Internet of Things [320].

Device Operating Systems (OS) and Hardware

The data set analyzed here shows that the investigations used different IoT devices (end devices and gateway devices), operating systems (OS), and hardware. Figure 2.11 shows the top authors' keywords per year for the most employed OS and hardware. Android is the most used OS for researchers, with 87 documents. This OS is used for IoT gateways [321–324] or end sensing devices [325–327]. Contiki is a lightweight OS for memory constrained systems (like microcontroller-based systems) designed for low-power wireless devices [328]. A total of 56 publications were found related to this OS, where the author uses capabilities like embedded protocols: 6LoWPAN [249,329], CoAP [330], and RPL [331]. In addition, some publications use the Contiki network simulator Cooja to simulate routing protocols [332] and performance evaluation [333].



(a) (b)

Figure 2.11: IoT devices operating systems
Internet of Things devices operating systems (OS) and hardware based on authors' keywords, for the period 2006 to 2016. (**a**) most used operating systems in authors' keywords per year; (**b**) most used hardware in authors' keywords per year.

Other operating systems, such as Linux, are used in IoT for image processing [334] and gateway services [335]. The iPhone Operating System (iOS) is used as user interface for presentation, configuration, and remote controlling for IoT environments [336]. Finally, last year, Culic et al. demonstrated the potential of Windows 10 IoT Core (Redmond, WA, United States), a lightweight version of Windows 10, as an IoT operating system optimized to run on small devices that have no display [337].

On the hardware side, some authors' keywords detail the hardware devices employed (see Figure 2.11b). Raspberry Pi is a small single board computer (SBC) capable of supporting operating systems like Linux Ubuntu, Windows, or Android. The Raspberry Pi is the most popular platform employed for IoT, with 88 publications, as a versatile platform for a gateway [338–340] or monitoring system [341,342]. Arduino boards are single-board microcontroller kits, in which the developer connects sensors, actuators, or RF communication interface easily using shield boards. For this specific IoT publications data set, 83 documents refer to Arduino hardware. These boards are widely used for IoT learning [336,343,344] and monitoring devices [345–347].

Presently, smartphones are highly capable embedded systems that run full OS, with integrated sensors. Sixty-six documents were found related to smartphones in IoT, be they used as sensors [348,349], gateway [350–352], or user interface [353,354]. The Field-Programmable Gate Array (FPGA) is a hardware reconfigurable component that contains an array of computational (logic) elements, with a functionality specified by a hardware description language [355]. These FPGAs are used in IoT investigations for data encryption [356–358], routing algorithms [359], and parallel simulation [360]. A microcontroller (MCU) is a small computer on a single integrated circuit, which includes a processor core, RAM/ROM memory, peripherals, and, in some cases, RF transceivers. For IoT, the MCU plays a fundamental role in sensing end devices [338,361,362] and actuators [363].

Top Trending Topics

For this analysis, the top trending topics are the authors' keywords, which have higher average growth rate (AGR) over the others. These topics represent concepts that have a large impact on IoT research. To find these trending topics, two-year AGR time periods (2011–2012, 2013–2014, and 2015–2016) were found.

Figure 2.12 shows the top eight trending topics with the AGR time periods. Cloud computing leads, with an AGR of 90 publications/year for 2015–2016, 284 documents on 2016, and a constant growth in all time periods. In 2013, Gubbi et al. mentioned that the integration of IoT with Cloud computing applications can enable the creation of smart environments such as Smart Cities and others [1]. The growth of publications about IoT related to Cloud computing shows that the mentioned integration is currently happening. The second trending topic on this list is security. This topic has a moderate growth in 2011–2012 and 2013–2014 periods (about 18 publications/years), but, in 2015–2016, its growth soared to 83 publications/year. Security backs the industry's concerns about the user privacy and confidentiality [364, 365]. The same way that the communications protocols were analyzed in this paper by layers, Jing et al. divided the IoT into three layers (perception, transportation, and application layers) to analyze features and security issues of each [366].

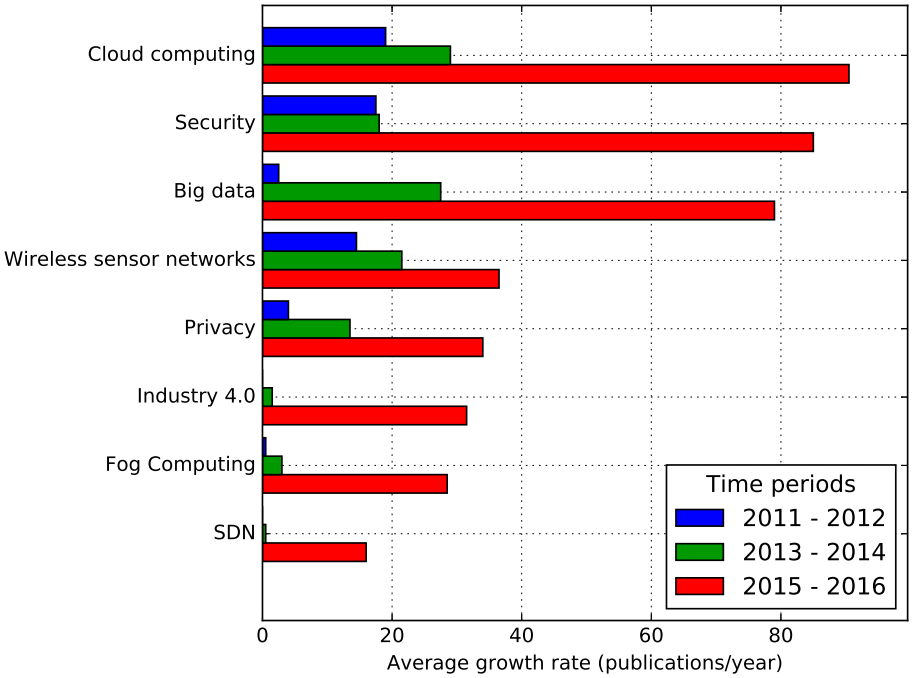


Figure 2.12: Internet of Things top trending topics based on authors' keywords, with average growth rate (AGR) for different times periods (2011–2012, 2013–2014, and 2015–2016).

IoT is one of many applications of Big Data because the rapid growth of IoT devices further propels the sharp growth of data to be processed and analyzed [142]. Wireless sensors networks (WSN), such as RFID, is one of the most important technologies enabling the IoT [367]. Likewise, security/privacy is a trending topic and also a concern in IoT, which was well summarized in [368].

Industry 4.0 is a new trending topic, without any growth in the 2011–2012 period, but with a sharp rise in publications from 3 to 66 in 2014 to 2016. Industry 4.0 includes the use of intelligent manufacturing processes, Cyber-Physical Systems (CPSs), and implementation and operation of smart factories [369]. This fourth industrial revolution aims to integrate IoT technologies such as remote control, manufacturing analytic tools and services, supply chains integration, and tracking and tracing inter- and intra-plant logistics [370]. Fog computing is also a new trending topic, with a small growth in 2011–2014 periods, but a large increase in the 2015–2016 period. Fog is a platform that provides compute, storage and networking services between end devices and cloud computing servers, most commonly, but not exclusively, located at the edge of network [132]. For IoT, this new platform is aimed to decentralize the data processing [371], decrease the latency [372], and bring more reliability for WSN [373]. Finally, Software-Defined Networking (SDN) is a novel concept for IoT, without any growth in the 2011–2012 period, but which was gaining popularity from one publication in 2013, and 2014, to 33 in 2016. SDN brings network routing intelligence via a centralized controller that connects to the network switch through the OpenFlow protocol [374], for example. This allows efficient node mobility [375], resource management [376], and improves the security of IoT networks [374, 377, 378].

2.3 FPGA

A Field Programmable Gate Array (FPGA) is a general purpose programmable logic device that contains logic blocks whose interconnection and functionality can be configured by a customer or a designer after manufacturing [379]. In this way, we can build inside an FPGA from a simple logic gate to a complex systems on chip or even a artificial intelligence system. As a result, FPGAs have been used for many different application such as digital signal processing [380–382], image processing [383–385], cryptography [386–388], parallel processing [389,390], fault tolerance systems [391–393], low power systems [394, 395], simulation [396–398], digital control [399–401], artificial inteligence [402–404], networking [405, 406], big data [407–410], among others.

Nowadays, we found several literature review and survey papers for different FPGAs applications like industry [411–413], power electronics [414], fault tolerance [392, 415–417], partial reconfiguration [418], photovoltaic systems [419], sensors system based [420, 421], network infrastructure security [422], LDPC (low-density parity-check) decoders [423], CORDIC algorithms [424], cryptography [386, 425], deep learning, [426–429], digital modulation techniques [430], low power design [431], robotic controllers [432], automotive safety [433], digital filters [434, 435], Unmanned Aerial Vehicles (UAV) [436,437], and random number generators [438]. Similarly, we found books that summarize FPGAs' applications for scientific research [439, 440]. These previous studies found in the related papers show the review of specific topics inside FPGA applications, and the related books review some FPGAs' applications with practical examples, but do not include the top applications like image processing, and machine learning.

2.3.1 Dataset collection

We built the dataset using two bibliographic databases: Clarivate Web of Science (WoS), and Scopus. The search string for this analysis was: "Field-programmable gate array*" OR "Field programmable gate array*" OR "FPGA*". We applied this string to the topic search in WoS and Scopus, which includes title, abstract, author's keywords, and KeyWords Plus® (for WoS). With this search criteria, we downloaded the data set within a day on 19th March 2019. Then, we preprocessed it in ScientoPy. Figure 2.13 shows the preprocess brief graph that presents the entire loaded documents for each database and the removed duplicated documents, respectively. Since the ScientoPy preprocessing script keeps WoS documents over Scopus documents, after the duplication removal, we see more documents from WoS than Scopus databases.

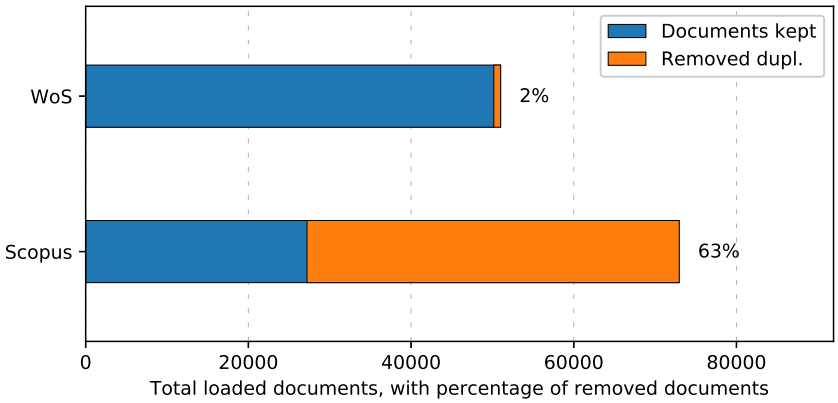


Figure 2.13: FPGA total loaded documents from Clarivate Web of Science (WoS), and Scopus databases, with the percentage of removed documents after duplication removal filter.

Table 2.13 shows the brief preprocessing table generated by ScientoPy. This table describes the input dataset including in the second column (*Number*) the number of publications after and before the duplication removal filter per database, and the third column (*Percentage*) the relative percentages (see table description for detailed information about these percentages). *Loaded papers* represents the total number of documents loaded from both databases. *Omitted papers by document type* are the number of documents outside the default documents type filter (only including conference papers, articles, reviews, proceedings papers, and articles in press). *Papers after omitted papers removed* are the number of documents inside the default documents type filter. *Loaded papers from WoS/Scopus* are the number of documents from each database after the omitted papers had been removed. *Duplicated papers found* are the duplicated total number of documents that have been found and removed. *Removed duplicated papers from WoS/Scopus* are the number of documents removed from each database after the duplication removal. *Total number of papers after rem. dupl.* are the number of documents after duplication removal by the preprocessing. Finally, *Papers from WoS/Scopus* are the whole number of documents from WoS and Scopus, respectively, after the duplication removal. The duplication removal filter used by ScientoPy is based on the DOI match or if the DOI is not present in the documents' title and documents' first author last name match.

Table 2.13: FPGA dataset preprocess brief table. *Omitted papers by document type*, *Loaded papers from WoS/Scopus* and *Duplicated papers found* percentage relative to *Loaded papers*. *Removed duplicated papers from WoS/Scopus* percentages relative to *Loaded papers from WoS/Scopus* respectively. *Papers from WoS/Scopus* percentage relative to *Total number of papers after rem. dupl.*

Information	**Number**	**Percentage**
Loaded papers	127597	
Omitted papers by document type	3621	2.8%
Papers after omitted papers removed	123976	
Loaded papers from WoS	51010	41.1%
Loaded papers from Scopus	72966	58.9%
Duplicated removal results:		
Duplicated papers found	46592	37.6%
Removed duplicated papers from WoS	836	1.6%
Removed duplicated papers from Scopus	45756	62.7%
Total number of papers after rem. dupl.	77384	
Papers from WoS	50174	64.8%
Papers from Scopus	27210	35.2%

2.3.2 Review methodology

Manual scientific reviews such as systematic and literature reviews have limitations to cover a vast research area such as FPGAs based applications completely. For this reason, we used a scientometric review methodology. Using ScientoPy, we extracted and analyzed the top applications and implementations based in FPGAs [50]. We took the total 77 384 papers' bibliographic information to perform a scientometric analysis with ScientoPy to extract the first 5000 top author's keywords. Then, we extracted the author's keywords related to FPGAs' applications from this list to arrange them into eleven different categories (digital control, communication interface, networking, computer security, machine learning, digital signal processing, image and video processing, computer algorithms, other implementations, and other applications).

Then, we analyze in depth each category by extracting with ScientoPy the statistical graph corresponding to the most used author's keywords for each topic. In that way, for instance, in the Machine learning section, we got the ScientoPy statistical graph for the top author's keywords related to machine learning techniques developed in FPGAs. The author's keywords that we present in the graphs represent the group of similar author keywords that belong to the same topic, such as abbreviations, plural/singular words, or dashes between words. For example, in machine learning, we got the "support vector machine" phrase (enclosing: support vector machine, SVM, support vector machines) or in Computer security/Cryptography we got RSA (enclosing: RSA, Rivest-Shamir-Adleman (RSA), Rivest-Shamir-Adleman, Rivest Shamir Adleman).

For the topic trending analysis, we use here two indicators. The Average Documents per Year (ADY) that is the average number of documents published in each specific topic in the last three years (2016 - 2018). This indicator represents the topic absolute-number of publications growth and generally is high when we have a high positioned topic. Unfortunately, this is not a

good indicator of a new trending topic, in which absolute growth is generally low, but its relative growth is high. For these cases, we have the second indicator called Percentage of Documents in the Last Years (PDLY) that represents the percentage of documents published in the last three years (2016 - 2018) for a specific topic relative to the total number of documents published for this topic. Therefore, we extracted the statistical graphs from ScientoPy using these indicators, with graphs divided into two categories:

- **Parametric evolution graph:** this graph has two parts. The first part (left side) presents the accumulative number of documents (or papers) vs. the publication year of each topic (in this case author's keywords). With this graph, we can observe the starting year at the line's start and the total number of documents at the line's end. In some graphs, we put the Y-axes on a logarithmic scale to note the starting year of each topic easily. On the right side, we get the parametric plot. Here, we present the ADY and PDLY of each topic, to show the growth of the total number of documents (ADY) and the relative growth (PDLY) in the last years.

- **Trending bar graph:** if we need to analyze many topics in a specific section (usually more than ten topics), we use this kind of graph. Here we present the different topics in the Y-axis related to the total number of documents per topic in the X-axis with bars. Also, here we highlight in orange in the bar the documents published in the last three years (in this case 2016 to 2018), including the PDLY value.

Finally, for the analysis of the topics, we include the definition of each topic, the specific implementations or applications with FPGAs related to the topics, and the citation of the papers that includes the related implementation or application. Here, we cited the most relevant to the application, the ones with more citations, and the newest papers for each specific application.

2.3.3 Digital control

Digital control uses digital systems to act as system controllers to control a system in an optimum manner without delay or overshot and ensuring stability [441]. Implementation of this kind of controllers in FPGAs allows highly parallel, high-speed processing, and shorter delays. Most of the documents listed here are related to fuzzy control and Proportional Integral Derivative (PID) control. Nevertheless, sensorless control has the highest PDLY, and model predictive control has the highest ADY (see Figure 2.14). Fuzzy control has been implemented in FPGAs to comply with the requirements of high-sampling-frequency control systems such as permanent-magnet synchronous motor drives [442], vehicle semi-active suspension system [443], or Continuous Variable Camshaft Timing (CVCT) system [444]. PID implementations in FPGAs allows high-speed and high-precision systems developed for DC-DC voltage converters [445, 446], nuclear fast reactors [447], and even for the controller of the magnetic suspension mass comparator system (MSMC) used for the redefinition of the kilogram at the National Institute of Standards and Technology [448].

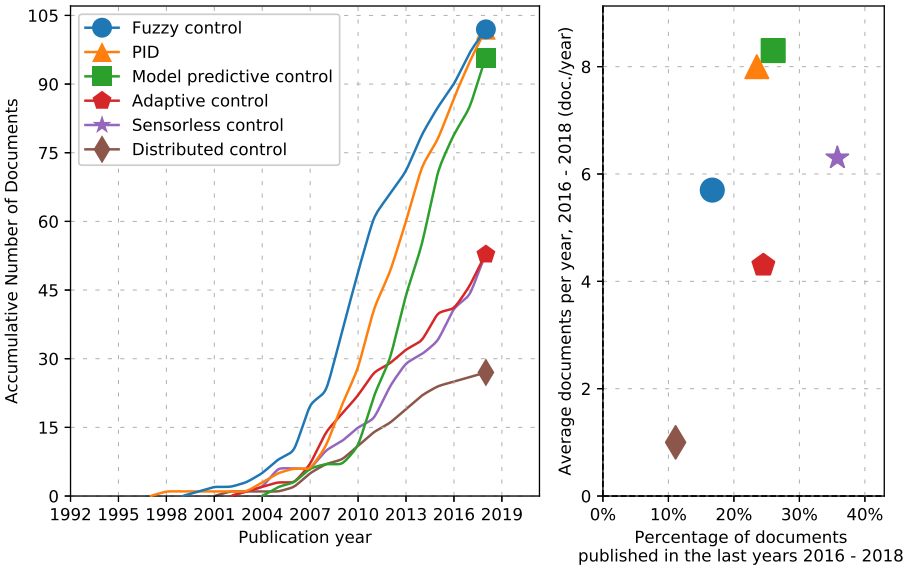


Figure 2.14: Digital control top implementations in FPGAs' research

The Model Predictive Control (MPC) uses a model to predict the process output at future time instants to calculate a control sequence for minimizing an objective function [449]. MPC is a quadratic programming (QP) problem, where two critical factors determine the success of MPC applications: the availability of a suitable plant model, and the ability to solve the quadratic programming problem within the prescribed sampling period [450]. The QP implementation in FPGAs provides an accurate real-time closed-loop simulation that meets the control deadlines [451]. This kind of implementations includes torque control at very low and zero speed [452], three-phase inverters [453, 454], or spacecraft rendezvous in elliptical orbits [455].

In the adaptive control, the controller adapts to a controlled system with parameters that can vary or are uncertain, such as an airplane where its mass change as a result of the fuel consumption [456]. These control systems have been implemented using FPGAs in robotics applications [457–460], tunnel lighting systems [461], microgrids [462], and chaotic systems [463, 464]. Sensorless control publications involve, for example, electrical motor speed and position control techniques that do not need a physical sensor. These techniques estimate the rotor position and speed by using algorithmic estimator techniques divided into two: the high-frequency injection method and the estimation-based techniques [465]. The estimation-based techniques use the Extended Kalman Filter (EKF) for position estimation due to its ability to extract the needed data from a random-noisy environment [466]. Real-time system based on FPGAs are used to implement the EKF matrix operations [466], vector controller [467, 468], and FPGA's oversampling technique for a flux observer [469–471].

Distributed control techniques are designed to process decentralized systems for distributed cells, where each cell processes different types of information. Each cell has autonomy in local optimization, and also, all integrate a large complex system [472]. FPGA-based distributed control techniques have been used for applications like micro-electromechanical systems arrays for air-flow planar micro-manipulation [473], music playing robots [474–476], telescopes control [477], and for reconfigurable FPGA-based systems [478–480].

2.3.4 Communication interfaces

The communication interfaces allow the data transmission and reception between the FPGA-based systems and its peripherals or storage devices. For this review, we have divided these interfaces into two (parallel and serial interfaces).

Parallel

Parallel communication interfaces in FPGAs are used for high speed data acquisition, communication protocols, and memory interfaces. As seen in Figure 2.15, the most used case are the image and video capture interfaces. First, the Charge-Coupled Device (CCD) is an image sensor used for different kind of applications (image [481], video [482], x-rays [483], and astronomical [484]). FPGAs' implementations has involved the CCD interface for high speed data acquisition [485–487], noise reduction [488, 489], ultra-high resolution [490, 491], among others. CMOS image sensors interface are also widely implemented in FPGA for high frame rate processing [492, 492, 493], exposure control [494–496], and dynamic range [497, 498].

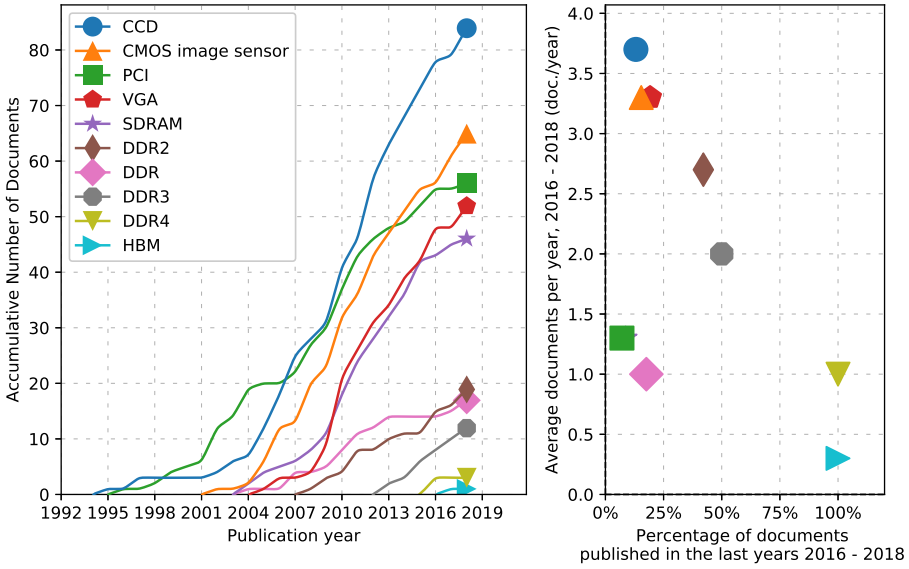


Figure 2.15: Parallel communication interfaces top implementations in FPGAs' research

PCI (Peripheral Component Interconnect) is one of the older interfaces used for FPGA communications. According to Figure 2.15, publications related to this topic started in 1996 [499], and finished in 2016, due this interface was replaced by the PCI Express. The VGA (Video Graphics Array) implementations include video and color scaling [500,501], video capturing [502], and real-time display [503, 504].

The memory interfaces for FPGAs have grown in a similar time that these interfaces have emerged. For instance, in 2004, the FPGAs were used for monitoring the SDRAM (Single Data Rate Synchronous Dynamic Random-Access Memory) data retention under electromagnetic irradiation environments [505,506]. The DDR (Double Data Rate) implementation also started in 2004 with the design of a memory scheduler [507]. DDR2 implementations started in 2008 with the design of a high-speed camera system, capable of capturing 500 frames per second [508].

DDR3 documents started in 2013 with the design of a 3D volumetric display system, which uses the DDR3 memory as a high-capacity high-bandwidth video frame buffer [509]. DDR4 implementations started in 2016, with the study of thermal and energy-efficient in the memory interface design for 28nm FPGAs [510,511]. Finally, in 2017, Gandhi et al. show the integration challenges for FPGA and HBM (High Bandwidth Memory) via an interposer interface [512]. These last two implementations (DDR4 and HBM) have 100% of PDLY for the last three years, which indicates that they are trending topics for the last three years.

Serial

Drive to higher bandwidth interfaces in computing devices has resulted in a major adoption of the serial communication interfaces [513]. That also has been reflected in FPGAs' research. Figure 2.16 shows a high increase in publication related to serial communication interfaces. Implementations for Ethernet physical layer in FPGAs are popular nowadays in next-generation Gigabit Ethernet implementations [514,515]. Also, precision delay measurement techniques have been developed to support the IEEE 1588 Precision Time Protocol [516–520]. Similarly, a security network processor was developed using FPGA for high-performance online security protocols processing [521,522].

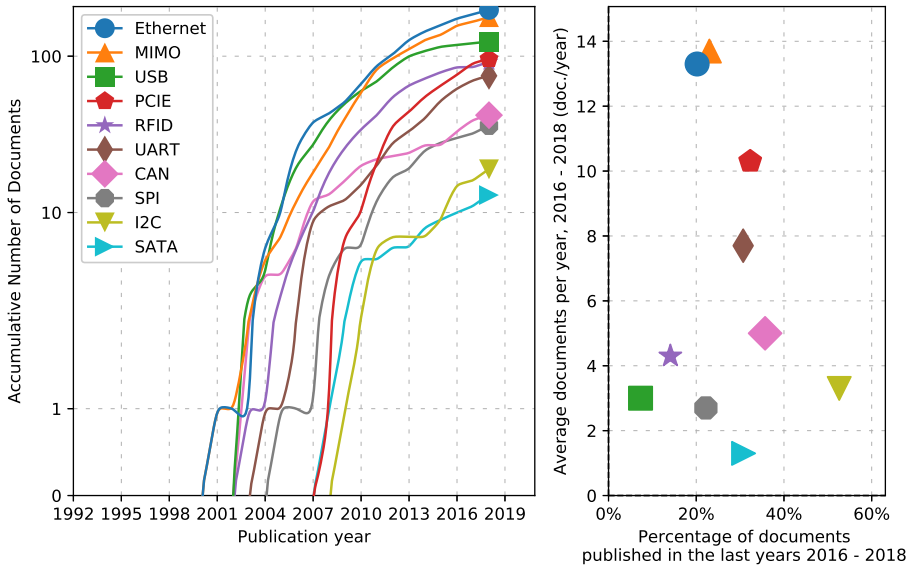


Figure 2.16: Serial communication interfaces top implementations in FPGAs' research

The multiple-input and multiple-output (MIMO) is the communication method implemented in FPGAs' research with the highest ADY. FPGAs allows real-time MIMO-OFDM (MIMO Orthogonal frequency-division multiplexing) transceivers implementations for multiple streams [523–525]. Also, channel estimation for MIMO uses FPGAs for efficient hardware resource utilization [526] and fast prototyping algorithms [527,528]. The USB (Universal Serial Bus) interface has been widely used for FPGAs' boards to a host computer communications [529–533]. In the same way, some authors have built FPGA security systems for monitoring and detect USB cable attacks [534] and also for building cryptography systems to add security in USB devices [535].

PCI Express (PCI-E) is nowadays the most used interface for high-performance communication between FPGAs and host-CPU (host - Central Processing Unit) [536, 537], GPUs (Graphic Processing Units) [538, 539], or other FPGAs [540, 541]. On the other hand, other researchers have worked with FPGAs and RFID (Radio Frequency Identification) for security analysis and RFID new implementations [542–544], hardware UART (Universal Asynchronous Receiver-/Transmitter) implementation and simulation [545–547], CAN (Controller Area Network) bus routers [548] and gateways [549]. SPI (Serial Peripheral Interface) and I2C (Inter-Integrated Circuit) communications are mostly used for FPGA to MEMS (Microelectromechanical systems) communications [550, 551, 551]. Finally, SATA (Serial Advanced Technology Attachment) interface has been implemented in FPGAs for high-speed data storage [552–554].

2.3.5 Networking

According to our dataset, the FPGAs have been used for networking applications since 1994. Figure 2.17 shows the top FPGA-based applications for networking. In Software Defined Radio (SDR), the components that have been traditionally implemented in hardware (such as mixers, filters, and modulators) are instead implemented in software (computers or embedded systems) [555]. The SDN (Software-Defined Networking) implementations based on FPGA includes OFDM modulators [556, 556–559], BPSK (Binary Phase Shift Keying) modulators [560, 561], QPSK (Quadrature Phase Shift Keying) modulators [560, 562], GNSS (Global Navigation Satellite System) and GPS (Global Positioning System) receivers [563–566], CDMA (Code-Division Multiple Access) [567], and QAM (Quadrature Amplitude Modulation) modulators [568, 569].

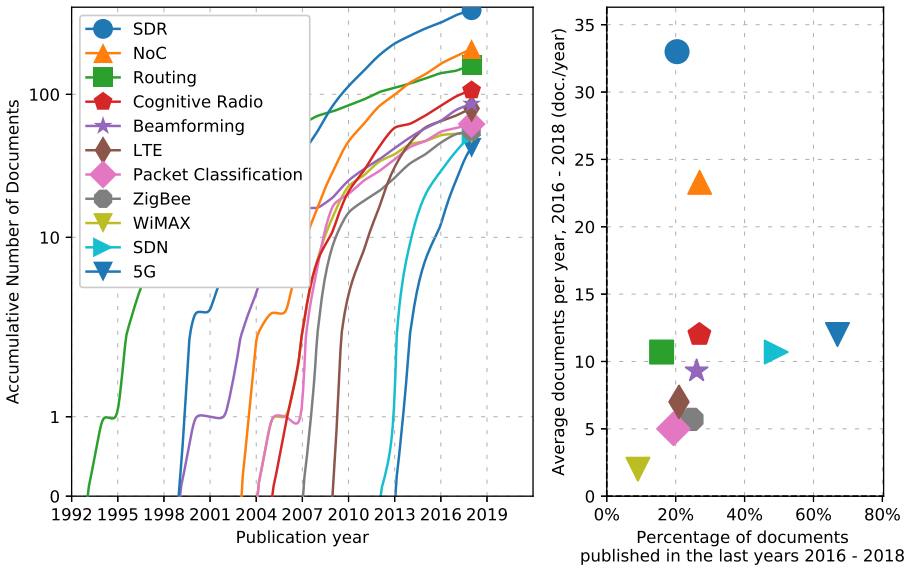


Figure 2.17: Networking top implementations in FPGAs' research

Network on chip (NoC) is a paradigm which aims to solve the communication issues between the CPU units of the next generation of many core System on Chip (SoC). Some FPGA-based implementations to solve NoC problems include network switches typologies [570–574,574], buffer handling [575, 576], router implementations [572, 577–582], and NoC simulators [583–585].

Routing applications are the first that have been implemented in FPGAs for networking, starting in 1994 [586]. These includes packet processing [587, 588], NetFPGA platform to prototyping networking devices (switches and routers) [589–591], and parallel routing [592–597]. Cognitive radio tries to solve the spectral congestion by using the best wireless channels in its vicinity to avoid user interference and congestion [598]. In this area, FPGAs have been using for spectrum sensing [599–612], reconfigurable antennas [613, 614], and adaptive codec [615]. Beamforming is a signal processing technique for directional signal transmission or reception in sensor arrays [616]. This keyword is correlated for FPGAs applications to beamforming in radio communications systems, and beamforming in ultrasound imaging. In this section, we are analyzing the first one. For radio communications systems, beamforming applications with FPGAs consist of band Infinite Impulse Response (IIR) beam filters [617, 618], and beamforming Direction Of Arrival (DOA) estimation [619].

Long-Term Evolution (LTE) applications related with FPGAs started in 2010 [620, 621], and these include the implementation of the Physical Downlink Shared Channel (PDSCH) [622, 623], Physical Downlink Control Channel (PDCCH) [624, 625], efficient implementation of a parallel-pipelined configurable FFT/IFFT (Fast Fourier Transform / Inverse Fast Fourier Transform) processor [626–629]. FPGAs play a crucial role in networking packet classification, because, due to the scalable and parallel models than can be built inside these systems, efficient and high-speed packet classification systems have been designed [630–634]. These systems have been applied to firewalls [635, 636], and OpenFlow capable switches [637]. ZigBee is a high-level communication protocol based on the IEEE 802.15.4 standard used in personal area networks such as home automation, smart farming, and other low power and low bandwidth applications [638]. FPGAs' applications in this protocol includes more efficient ZigBee transceivers and MAC (Medium Access Control) protocol implementations [639–643], and data encryption in security improvement for ZigBee networks [644–646]. 5G (5th Generation) is the latest generation of cellular mobile communications that aims at the high data rate, improve the latency and the energy-saving [647]. WiMAX (Worldwide Interoperability for Microwave Access) is a wireless technology to provide last mile Internet broadband access [648], and it was a candidate for 4G communications, in competition with LTE. FPGAs implementations for this technology includes OFDM transceiver [649, 650], SDR [651–653], and Viterbi decoders [654–656]. Nevertheless, WiMAX lost the competition for 4G. As a result, we see it as the lowest ADY on this list. Software-Defined Networking (SDN) is a network management approach that enables programmatically efficient network configuration to improve network performance and monitoring [657]. For SDN we can find implementations in FPGA related to ultra low latency data center services [658], Software Defined Hardware Counters (SDHC) for dynamic network statics [659], high speed network (10Gbps) performance evaluation [660], packet arrival time measurement [661], and anomaly-based intrusion detection [662]. Similarly, as for SDR, in SDN we found several implementation based on NetFPGA platform [590, 660, 661, 663–668]. FPGAs' applications for 5G have the highest PDLY (see Figure 2.17). These applications have helped to enable this new technology from 2014 with implementations like the antenna testbed for massive MIMO [669, 670], transceiver modulator/demodulator enablers [671–674], time delay and latency estimation [675, 676], and beam direction of arrival estimation [677]

2.3.6 Computer security

Computer security or cybersecurity aims to protect confidentiality, integrity, and availability of data and assets used in cyberspace [678]. Figure 2.18 shows the top FPGAs' applications for computer security with their number of documents and the PDLY. The first one is fault tolerance with near to 400 documents. This is a feature that enables a system to continue operating properly in the event of a failure [679], and it is widely used for space [680–685], automotive [686,687], and robot controllers applications [688,689]. NASA defines Single Event Upset (SEU) as "radiation-induced errors in microelectronic circuits caused when charged particles (usually from the radiation belts or from cosmic rays) lose energy by ionizing the medium through which they pass, leaving behind a wake of electron-hole pairs". Then SEUs are random software errors of a transient nature in integrated circuits but are not generally non-destructive to hardware [690]. FPGAs have been used to built fault tolerance systems against the SEU [691–694]. Another security topic is fault injection, which involves inserting faults into a particular target at a determined time in the process and monitoring the results to determine its behavior in response to this generated fault [695]. Implementations of this kind in FPGAs help to efficiently analyze the performance of fault tolerance systems [695–699].

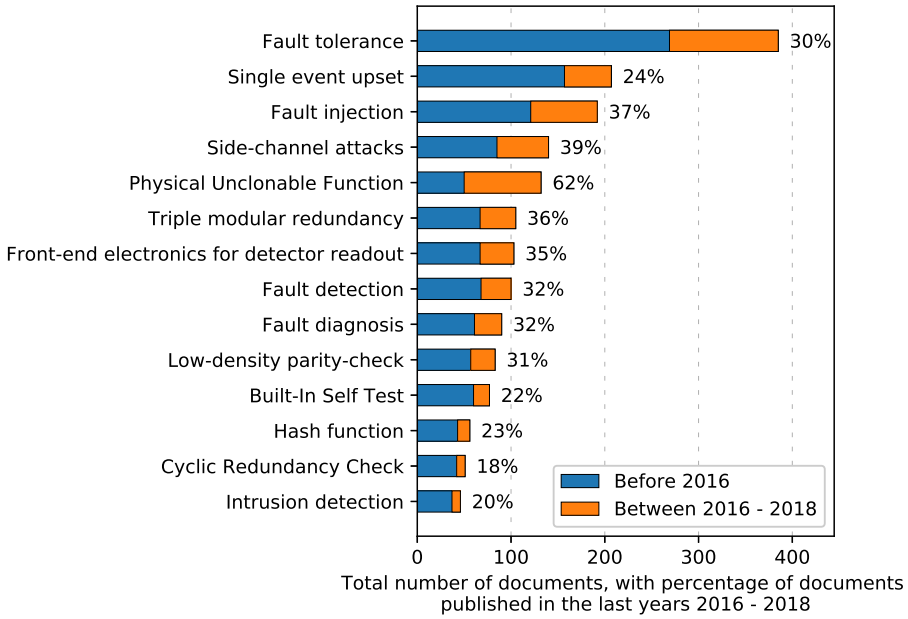


Figure 2.18: Security top applications in FPGAs' research

Side-channel attacks (SCA) refers to any attack based on information leaked for a cryptographic module that performs encryption or decryption of secret parameters via power dissipation, electromagnetic radiation, or operating times as side-channel information [700]. FPGAs' research in this area covers FPGAs' vulnerabilities to SCA [701, 701–703], security resistant designs against SCA [704–709], and hardware Trojan detection [710–712]. Physically Unclonable Function (PUF) is a noisy function that when queried with a challenge x, it generates a response y that depends on both x and the unique device-specific intrinsic physical properties of the object that contains the PUF [713]. In that way, the PUF is used as a digital fingerprint to

identify a semiconductor device. FPGAs' applications for PUF have the highest PDLY (62% of the documents published in the last three years), and these includes Ring Oscillator (RO) based physical unclonable function [714–718], and PUF strong evaluation [719–722].

Triple Modular Redundancy (TMR) is a fault-tolerance method, in which at least three systems perform a process, and the result is processed by a majority voting system to produce a single output [723]. FPGAs are the perfect system to implement TMR due to its parallel design architecture. Applications of TMR in FPGAs covers novel design techniques of TMR [724–727], and TRM SRAM based systems [728–730], among others. FPGAs' systems can capture and process information at a very high speed compared with conventional systems. For this reason, FPGAs' systems have been widely used as front-end electronics for detector readout calorimeters [731–733], neutrino detectors [734,735], and even particle tracking systems for the Large Hadron Collider (LHC) [736–740].

Other applications in our top list related to FPGAs are fault detection systems [741–746], fault diagnosis [747–752], Low-Density Parity-Check (LDPC) implementations for error correcting code in transmission [753–756], magnetic storage systems [757, 758], Built-In Self Test (BIST) [719, 759–763], hash function implementations [764–769], parallel and high speed Cyclic Redundancy Check (CRC) implementations [770–773], and efficient intrusion detection systems [774–779].

Cryptography techniques

Cryptography techniques are created for securing digital information, transactions, and distributed computations from third parties or the public that attempt to read private messages [780]. Figure 2.19 shows the top FPGAs' cryptography techniques implementations. Advanced Encryption Standard (AES), also know as Rijndael, is the most popular encryption technique that researches have implemented in FPGAs, with 510 documents. These implementations have been made to increase the encryption speed [781–785], generate small footprint and cheap designs [544, 786, 787], test the encryption against fault injections/attacks [788, 789], and to improve the fault detection/tolerance systems [741, 790, 791]. Elliptic Curve Cryptography (ECC) is increasingly used in practice to instantiate public-key cryptography protocols, based on the algebraic structure of elliptic curves over finite fields [792]. In FPGAs' cryptography applications, it has the second ADY, with an average of 27 documents per year (2016 to 2018). FPGAs' implementations of these cryptography techniques includes efficient ECC processors [793–795], side-channel attack resistant implementations [704, 706], and high speed implementations [796, 797].

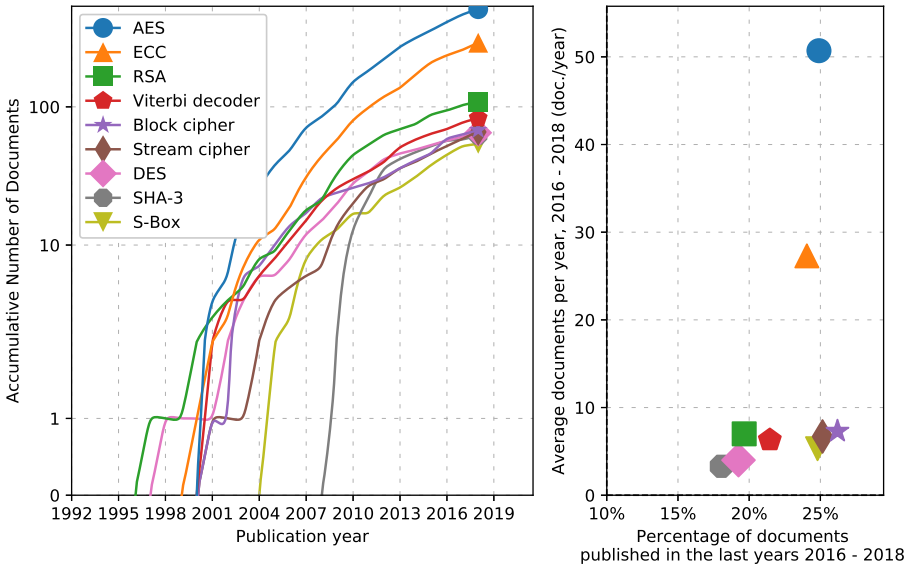


Figure 2.19: Cryptography top implementations in FPGAs' research

RSA (Rivest–Shamir–Adleman) is one of the first public-key cryptography algorithm, and it is based on the practical difficulty of the factorization of the product of two large prime numbers [798]. For RSA we found different FPGAs' implementations such as efficient or accelerated architectures [799–801], side-channel attacks resistant [802, 803], tiny footprint [804], and Vedic mathematics based implementation [805]. Other cryptography techniques implemented in FPGAs are the Viterbi decoder with reconfigurable capabilities [654], high speed Viterbi decoders [806, 807], steam cipher chaos-based techniques [808–811], and lightweight block cipher [812–814].

The Data Encryption Standard (DES) is an old encryption standard that is insecure for modern applications, but has influenced in the advancement of modern cryptography [815]. FPGAs have been used to built cryptanalysis to crack a DES key [815–817], for DES pipelined implementations [818], and speed/power efficient implementations [819–821]. In 2008, the NIST (National Institute of Standards and Technology) started the competition for the new cryptographic Secure Hash Algorithm (SHA-3) [822]. Figure 2.19 shows that the implementations in FPGAs for SHA-3 started in 2009 with test and comparatives for SHA-3 candidates [823–828]. On October 2012, the Keccak cryptographic function was selected as the winner of the competition [829], and then implementations for the Keccak SHA-3 started in FPGAs [830], such as high throughput/performance [831–834], IoT focused applications [832], and compact implementations [835]. Finally, S-Box (Substitution-Box) is a substitution transformation used to obscure the relationship between the key and a encrypted text [836]. S-Box technique has been implemented in FPGAs for high throughput processing [837–839], memory efficient [840–843], low latency [844], and low power implementations [845–847].

2.3.7 Machine learning

Machine learning is one of the top FPGA-based applications. Figure 2.20 shows the most implemented machine learning techniques for this architecture, where the neural network is the top one. These neural network implementations have been applied to pattern recognition [848–851],

photovoltaic optimizations [403], modeling [852, 853], controllers [854], and diagnostics [747]; power quality [855,856]; robotics control [857], robotics object detection and manipulation [858], and finaly robotics object seeking [859]. Secondly, genetic algorithm applications include image processing [860–863], task scheduling [864–866], frequency estimation for digital relaying in power electrical systems [867–870], and mobile robots path planning [871–874].

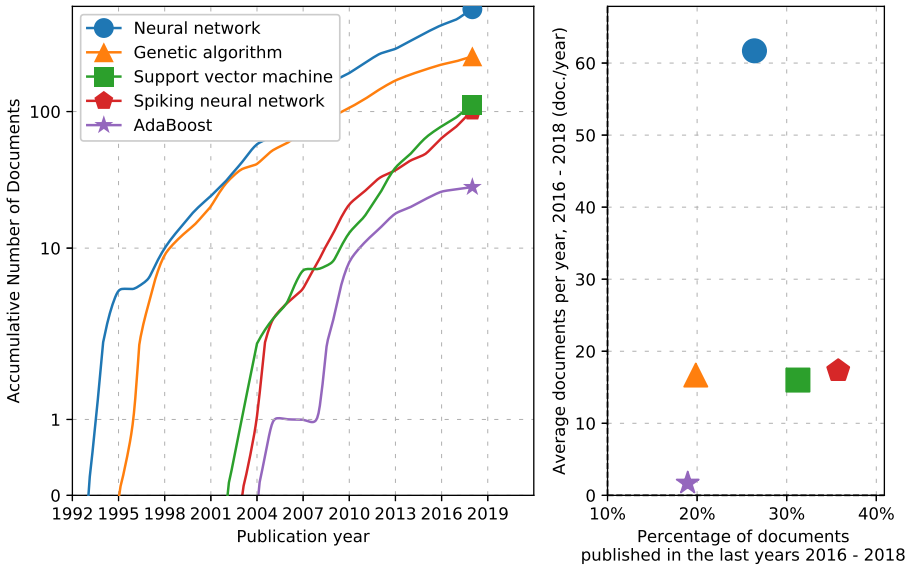


Figure 2.20: Machine learning top implementations in FPGAs' research

Support Vector Machine (SVM) are widely used for classification and regression analysis [875]. The implementation of this technique in FPGAs is one of the newest, starting in 2002 (see Figure 2.20). The SVM has been used in FPGAs alongside the Histogram of Oriented Gradients (HOG) for object classifications in image processing [876–880]. Other SVM applications include facial expression recognition [881–883], network traffic classification [884], melanoma detection [885–887], arrhythmias detection [888, 889], epilepsy detection [890], and stress detection [891].

The spiking neural networks are a more biologically realistic model, with spiking neurons that transfer the information in the precise timing of spikes or a sequence of them [892]. For FPGAs, this machine learning technology has the highest PDLY (51% in the last three years). Some applications of this technique in FPGAs include character recognition [893, 894], sound recognition [895,896], and other patterns/object recognition [897,898]. The AdaBoost technique (short for Adaptive Boosting) improves the performance of a weak learning and classifier algorithm into a strong one. This machine learning technique is the newest that has been implemented with FPGAs in our list (starting in 2005). It has been widely applied for image processing in face detection [899–903], and also for human detection [876, 904].

2.3.8 Digital signal processing

Digital Signal Processing (DSP) is the performing of signal processing using digital techniques by a computing device [905]. Figure 2.21 shows the top DSP techniques implemented in FPGAs without covering digital filters, which are covered in the next sub section. Fast Fourier Transform (FFT) is the most implemented DSP technique in FPGAs, with near to 677 documents related

to it. Here, we found CORDIC-based FFT [906–911], double-precision floating-point FFT [912], OFDM systems based in FFT [913–917], radix-2 FFT [918, 919], and radix-4 FFT [908, 920–922] implementations. The Discrete Wavelet Transform (DWT) is a wavelet transform by a certain orthonormal series generated by a discrete wavelet to capture both frequency and location information [923]. The DWT have been implemented in FPGAs for image and video compression [924–928], digital watermarking [929,930], EEG (Electroencephalography) signal processing [931–933], and general image processing [934–936].

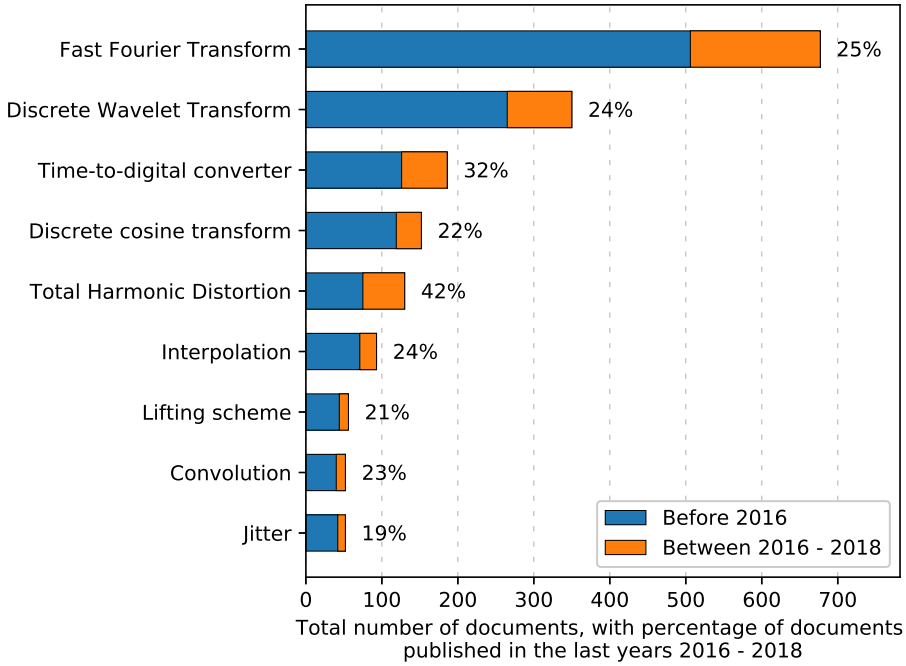


Figure 2.21: Digital signal processing top implementations in FPGAs' research

Time-to-digital converters (TDC) are designed to measure a time interval and convert it into digital output [937]. FPGAs' implementations of TDCs offer high accuracy in time measurement. These technique has been used for Positron Emission Tomography (PET) [938–941], Light Detection And Ranging (LIDAR) [942, 943], and high speed ADC (Analog-to-digital converter) [944, 945]. Discrete Cosine Transform (DCT) implementations in FPGAs have been applied to MPEG-based video encoders [946–948], JPEG encoders [949, 950], for the Pierre Auger cosmic rays observatory front end detectors [951–954], and recently to image mosaicing systems [955]. Total Harmonic Distortion (THD) is a measure of the effective value of the harmonic components of a distorted waveform, and it is commonly used for a quick measure of distortion [956]. THD implementations in FPGA have the highest PDLY in this category (43% of documents in the last three years), and these have been implemented in FPGAs for multilevel inverters [957–960], AC (Alternating Current) LED (Light-Emitting Diode) drivers [961–964].

Interpolation with FPGAs have been used for video scaling [965–967], and motion estimator for High Efficient Video Coding (HEVC) encoder [968–970]. Other digital signal processing implementations in FPGAs includes lifting scheme for efficient and modular DWT [971–974], efficient convolution techniques [975–977], and 3D convolution [978]. Finally, in our list is the jitter detection (deviation from true periodicity of a presumably periodic signal) using FPGAs

[979], which includes jitter studies for 5G communications [676], Multi-Gigabit FPGA-Embedded Serial Transceivers [980], clock oscillators [981], and random number generators based on clocks signal jitter [982–984].

Digital filters

A digital filter is a filter that operates on digital signals to perform mathematical operations to reduce or enhance certain aspects of that signal [985]. Figure 2.22 shows the top digital filters techniques implemented in FPGAs. Finite Impulse Response (FIR) filter is a filter where the output is computed as a weighted, finite term sum of past, present, and perhaps future values of the filter input [986]. FPGAs have been used for efficient implementation of FIR filters using distributed arithmetic [987–990], and for high speed/low power implementations [991–993]. The Kalman filter uses a series of measurements observed over time, which include statistical noise and other inaccuracies, to produce an estimate of unknown variables [994]. FPGAs were used for high performance/efficiency implementation of Kalman filters [995–997], IMU (Inertial Measurement Unit) sensors fusion [998–1000], and real-time filtering [1001–1003].

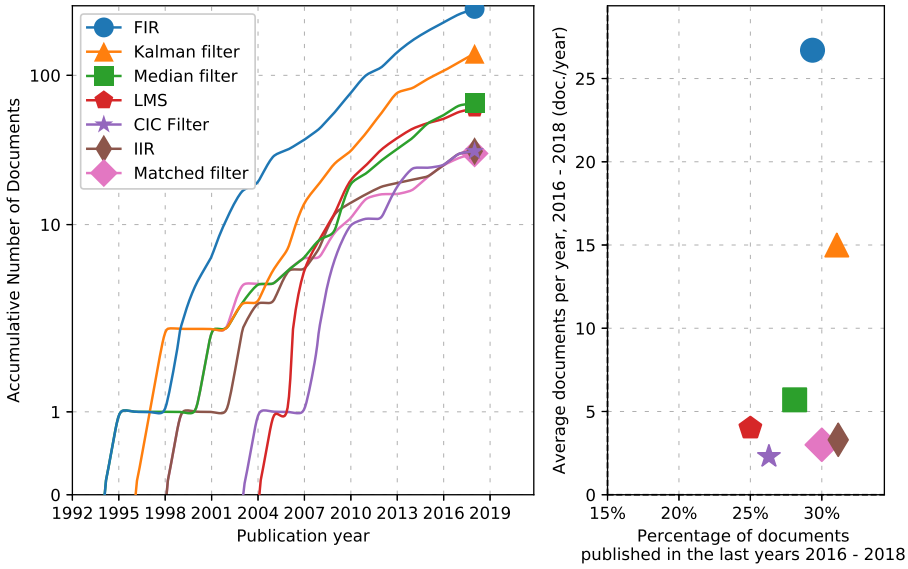


Figure 2.22: Digital filters top implementations in FPGAs' research

Median filters implementation in FPGAs includes application for image processing [1004–1007], low power median filters [1008, 1009], and high speed/real-time applications [1010–1012]. The Least Mean Squares (LMS) filter is an adaptive filter that finds the adequate filter coefficients to produce the least mean square error of the difference between the desired and the actual signal [1013]. The LMS filters have been used in FPGAs for active noise cancellation in headphones [1014], echo cancellation [1015–1017], and non invasive fetal ECG (Electrocardiogram) [1018, 1019]. Other digital filters implementations in FPGAs include Cascaded integrator–comb (CIC) filter [1020–1024], Infinite Impulse Response (IIR) filters [1025–1028], and matched filter [1029–1033].

2.3.9 Image and video processing

Image and video processing techniques comprise the use of computer algorithms to perform video/image acquisition, compression, preprocessing, segmentation, representation, extraction, recognition, and interpretation [1034]. These techniques involve one of the most important applications in FPGAs. Figure 2.23 shows the top image and video processing techniques implemented in FPGAs, without including image and video/image compression standards that we include in the following subsection. First, stereo vision tries to infer the scene geometry from two or more images taken simultaneously from slightly different viewpoints [1035]. This is the top image/video processing technique in FPGAs with 161 documents, and includes real-time stereo vision implementations [1036–1039], Census transform [1040, 1041], 3D reconstruction systems [1042, 1042, 1043], and even the use of this technique with FPGAs for the Mars rovers navigation systems [1044, 1045]. Face detection and recognition is the second topic in this list. Applications related to this topic in FPGAs include face detection with Haar classifiers [1046–1049], real-time/high speed face detection/recognition [1050–1055], AdaBoost based face detection [899, 902, 1056], and Viola-Jones based face detection algorithm [1057–1059].

Edge detection aims to identify points in an image at which the brightens or other image characteristics changes sharply. FPGAs' implementations for edge detection cover implementations based in Sobel operator [1060–1064], Canny algorithm [1065–1067], applications for real time processing [1068–1072], image segmentation [1073, 1074], DNA (Desoxyribonucleic Acid) microarray image processing [1075, 1076], and object detection [1077–1079].

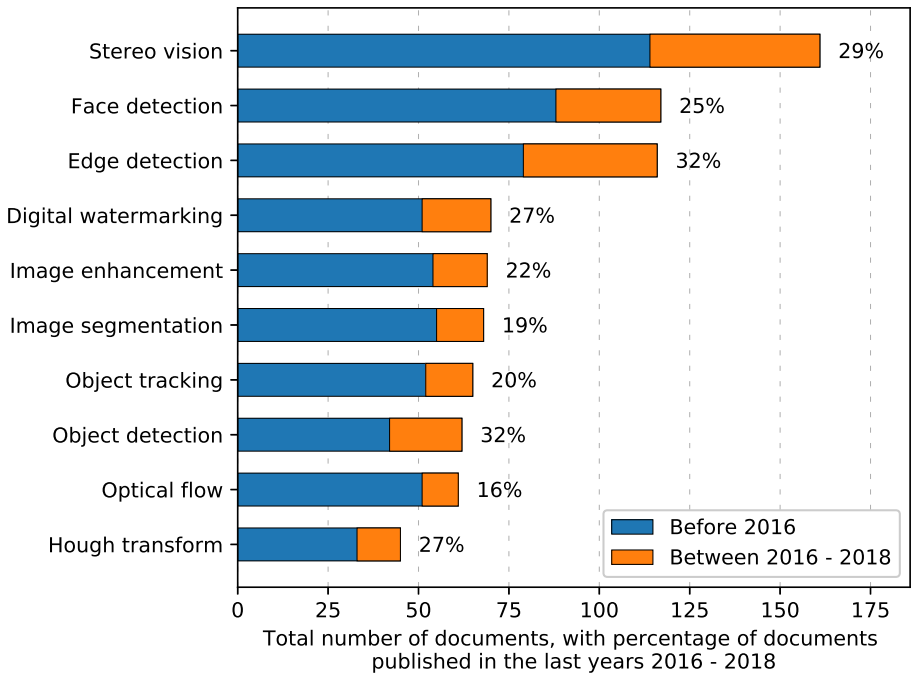


Figure 2.23: Image and video compressing processing top techniques implementations in FPGAs' research

Digital watermarking is the act of hiding information in multimedia data, such as image, video or audio, for content protection or authentication [1080]. FPGAs in digital watermarking have been used for real time watermarking detection in video [1081, 1082], Discrete Cosine Transform

(DCT) based digital image watermarking [1083–1085], and Discrete Wavelet Transform (DWT) based digital image/audio watermarking [930, 1086, 1087]. Image enhancement is used "to improve interpretability or perception of info available within the images, making it suitable for human vision, as well as to provide improved input to the other automated image processing techniques" [1088]. FPGAs' implementations for this technique include histogram equalization [1089–1092], retinex image enhancement [1093–1095], Infrared Focal Plane Arrays (IRFPA) image enhancement [1096, 1097], and telescopes' atmospheric turbulence mitigation [1098, 1099]. Other image processing applications that use FPGAs are image segmentation [1100–1104], object tracking [1105–1109], object detection [1110–1114] (real time object detection [1115–1117], moving objects detection [1118–1120], pedestrian detection [1121–1124], and background identification [1125–1127]), optical flow [1128–1132], and Hough transform [1133–1137].

Compression standards

Images and videos need substantial storage space. A single uncompressed 12 megapixels image with 24-bit color depth requires 36MB to be stored in PPM format (portable pixmap file format). A full HD video with 24-bit color depth, and 60fps requires 356MB/s ($(24/8)*1920*1080*60 = 355.957MB/s$), or 1.22TB/h. If that were the case, a 3Gbps Internet connection speed would be required to watch online full HD videos. For this reason, image and video codecs store the information with compression standards that reduce the required storage size significantly. FPGAs' implementations of these compression standards allow real-time coding of complex algorithms. To the present day H.264 is the most popular standard for video codding related to FPGAs' implementations (see Figure 2.24). The research of FPGAs' implementations for this codec started in 2003 [1138], and some implementations are related to motion estimation [1139–1143], intra-prediction [1142, 1144–1147], quantization [1148, 1149], and DCT (Discrete Cosine Transform) [1150, 1151].

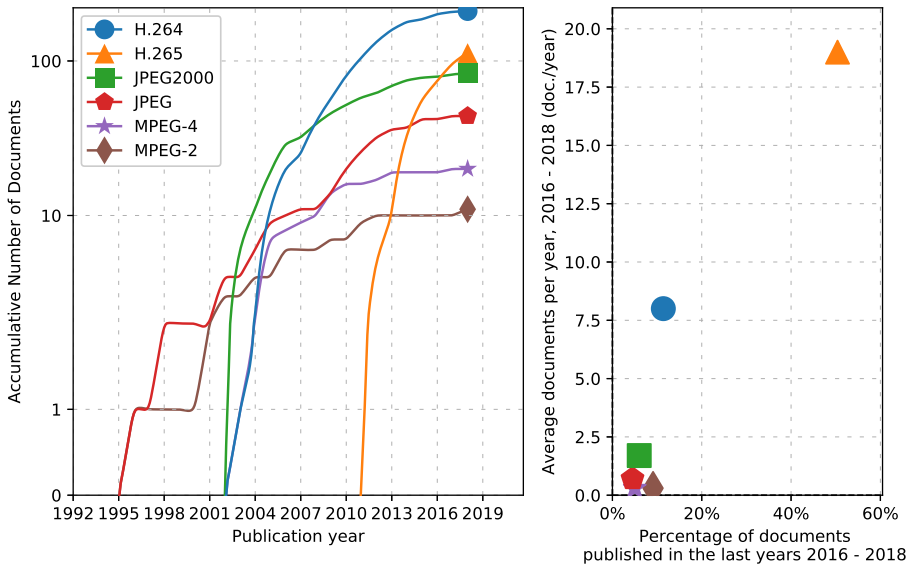


Figure 2.24: Image and video compressing codecs top implementations in FPGAs' research

High-Efficiency Video Coding (HEVC) or H.265 is considered the successor of the H.264

video codec for higher resolution video applications [1152,1153]. This new codec is doubling the compression ration of its predecessor [1154–1156]. FPGA implementations and tests of this codec started in 2012, and today has the highest ADY and PDLY (50% of the documents published in the last three years, see Figure 2.24). One of the most critical challenges for H.265 is the efficient implementation of CABAC (Context-based Adaptive Binary Arithmetic Coding) that the research community considered as a well-known throughput bottleneck due to its strong data dependencies [1157–1159].

MPEG-2 (Moving Picture Experts Group) implementations in FPGAs started in 1996 [1160], and MPEG-4 in 2003 [1161]. The MPEG-2's ADY is close to zero, which indicates that there have been almost no publications in this topic from 2016. Similarly, MPEG-4 has a low ADY of 0.3 documents/year, with research documents focused on the AAC (Advanced Audio Coding) implementation [1162–1164].

On the other hand, image compressing standards implementation in FPGAs started with JPEG (Joint Photographic Experts Group) in 1996 [1165]. JPEG2000 implementations started in 2003 [1166–1168] and surpassed JPEG the same year. JPEG2000 standard uses a wavelet-based method to provide better rate-distortion performance than the original JPEG [1169]. The embedded wavelet coding algorithm know as EBCOT (Embedded Block Coding with Optimized Truncation of bit-stream), used for JPEG2000 standard, has been widely implemented in FPGAs for parallel optimization [1170–1175].

2.3.10 Big data

Dumbill defines big data as the "data that exceeds the processing capacity of conventional database systems" [1176]. Big data systems are focused on analyzing efficiently this kind of data with not conventional systems, which are boosted by FPGA-based applications. Figure 2.25 shows the leading big data techniques evolution graph related to FPGAs' research.

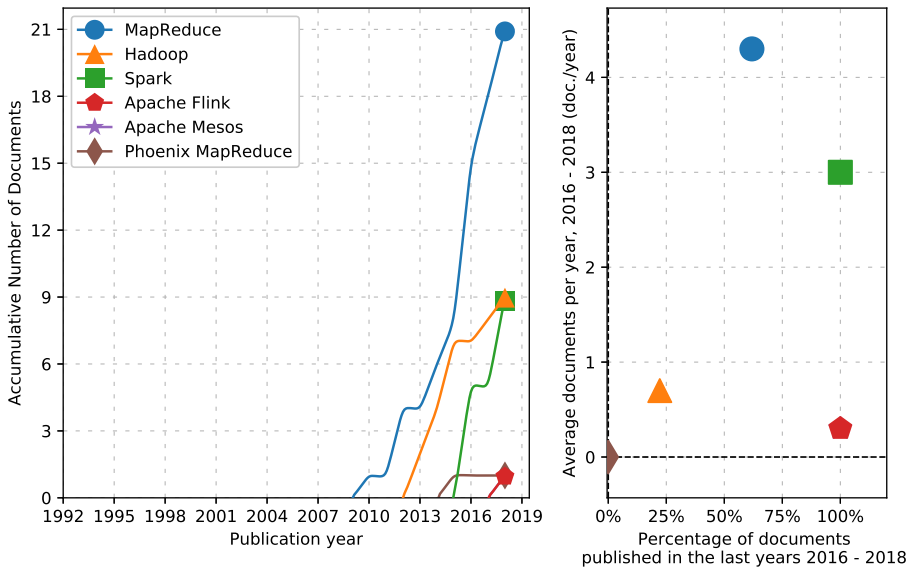


Figure 2.25: Big data top implementations in FPGAs' research

MapReduce is a programming model for processing and generating large big data sets with

a parallel or distributed algorithms [1177]. FPGAs have been used to accelerate MapReduce algorithms by different frameworks such as FPMR (FPGA MapReduce) [1178], MrHeter for heterogeneous data centers [1179], and Melia based on OpenCL [1180]. Other accelerators for MapReduce include scalable data center FPGA-based accelerators (HLSMapReduceFlow [1181]), coarse-grained reconfigurable architecture acceleration [1182], energy-efficient accelerators [1183, 1184], and others [1185, 1186]. Hadoop (also known as Apache Hadoop) is an open-source framework for distributed storage and distributed processing on huge data sets into computer clusters [1187]. For Hadoop, FPGAs' applications include energy-efficient acceleration of big data analytics [1184], FPGA-accelerated Hadoop cluster for deep learning computations [1188], process streaming data from SSDs (Solid State Drives) using FPGAs [1189], and low-power Hadoop cluster [1190].

Spark (also known as Apache Spark) is an open-source distributed general-purpose cluster computing system framework from Apache that supports in-memory computing, which enables it to process data faster compared to disk-based engines like Hadoop [1191]. FPGAs' applications related to Spark have the highest relative growth, with 100% of the publications in the last three years. For Spark, FPGAs have been used to accelerate the Spark process [409, 410, 1192], and deep convolutional neural networks for the Spark environment [1193]. Other big data frameworks accelerated by FPGAs are Apache Flink in heterogeneous hardware [1194], Apache Mesos for cluster management for the HetSpark framework [1195], and Phoenix MapReduce in multi-core FPGA's systems [1196].

2.3.11 Computer algorithms

FPGAs have a high capability to accelerate computer algorithms due to the parallel decomposition characteristics of some of them. This section shows the computer algorithms that are not enclosed in the previous sections. Figure 2.26 shows the top 10 algorithms implemented in FPGAs. CORDIC (for COordinate Rotation DIgital Computer) algorithm makes it possible to multiply and divide numbers by only shifting and adding steps. Also, it performs rotations to compute sine, cosine, and arctangent functions [1197]. The CORDIC algorithms implementations in FPGAs have been used for FFT processing [906,907,1198], OFDM [1199,1200], and DCT transform [1201,1202]. Hardware floating point implementations in FPGAs are common for high performance FFT applications [1203–1206], floating point based neural networks [1207,1208], and double precision floating point modules [1209–1212]. On the other hand, in Distributed Arithmetic (DA), multiplication is performed using precomputed lookup tables instead of the logic, reducing the cycles required to compute a final result [1213]. FPGAs' implementations of DA have been used for FIR filters [987, 988, 1214–1216], discrete cosine transform [1217–1220], and wavelet transform [935, 1221–1223]. Another FPGAs' computer algorithm implemented in FPGAs is the Smith-Waterman algorithm [1224–1227], and its implementation for DNA sequence analysis [1228, 1229].

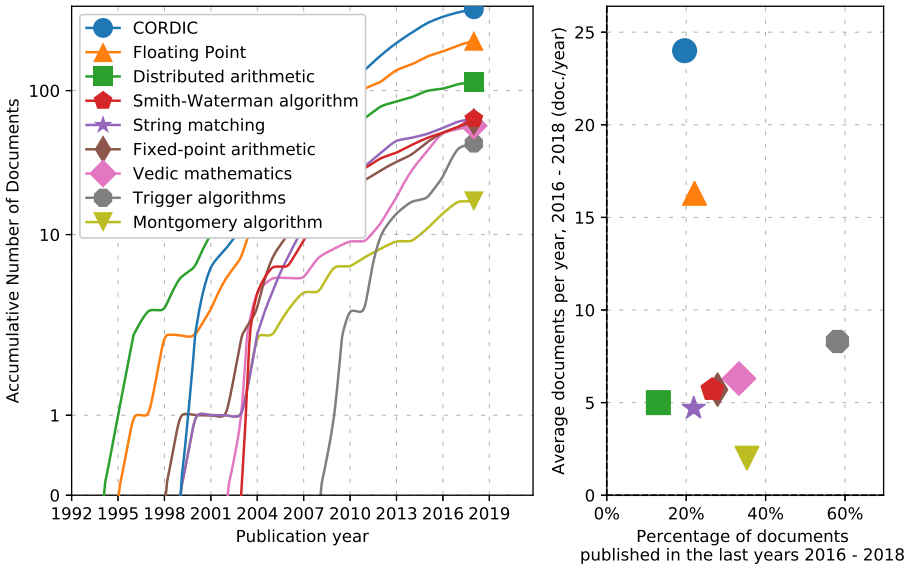


Figure 2.26: Top algorithms implementations in FPGAs' research

String matching algorithms tries to find the position where patterns are found within a larger string or text [1230]. For FPGAs we found string matching implementations for network intrussion detection [1231–1233], deep packet inspection [1234], and string matching algorithms based in bloom filter [1235, 1236]. Fixed-point arithmetic algorithms have been used in FPGA for accuracy-guaranteed bit-width optimization [1237,1238], Jacobi SVD (Singular Value Decomposition) [1239], Lanczos tridiagonalization [1240, 1241], and deep belief networks [1242, 1243]. Vedic mathematics is a system based on 16 sutras or aphorisms used for mathematical mental calculation operations [1244]. Vedic mathematics algorithms have been implemented in FPGAs for faster [1245–1248], and energy efficient [1249–1251] multiplication operations. Other algorithms implemented in FPGAs are the trigger algorithms [1252–1255], trigger algorithms for the ATLAS experiment [1256–1259], and Montgomery algorithm for cryptography applications [1260, 1261, 1261–1263].

2.3.12 Other implementations

Figure 2.27 shows other top implementation techniques in FPGAs' research. Pulse Width Modulation (PWM) technique is one of the most used strategies for controlling the AC output of power electronic converter by varying the duty cycle of a converter switches [1264]. FPGAs' implementations for PWM includes application for inverters [1265, 1265–1268], digital control for power converters [399, 1269–1272], and total harmonic distortion reduction [1273–1276]. A Finite-State Machine (FSM) is a representation of an abstract machine that can be or can change into a state that represents a possible situation. This change from one to another state is called transition, and occurs in response to an external input [1277]. Implementations of FSMs in FPGAs include low power FSMs [1278, 1279], and engineering education [1280, 1281].

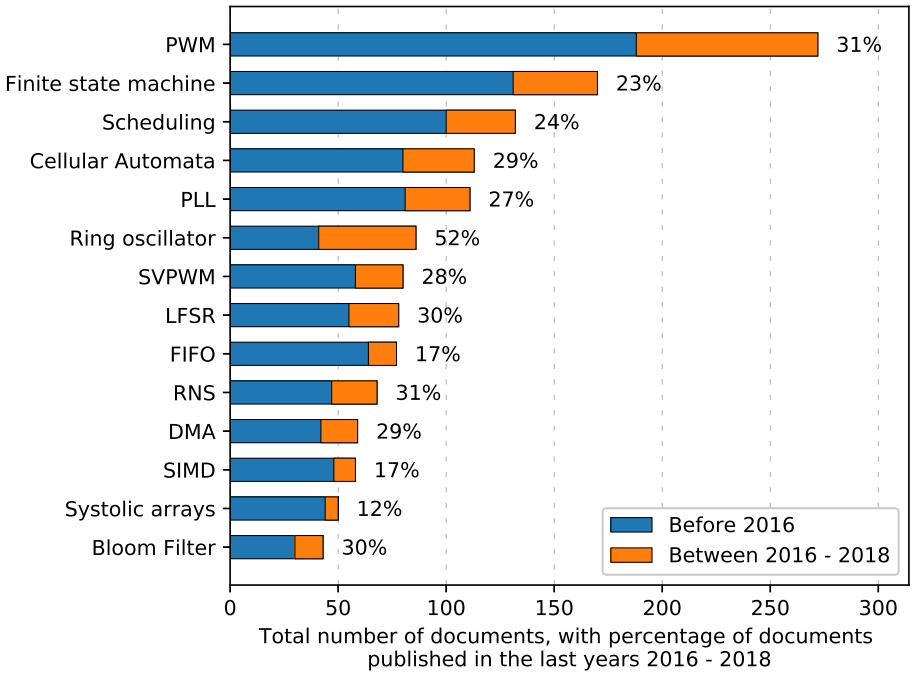


Figure 2.27: Other top implementations techniques in FPGAs' research

In computing, "scheduling is the method by which work is assigned to resources that complete the work" [1282]. Scheduling in FPGAs has been used for reconfigurable computing [1283–1285], real-time applications [1286–1288], and heterogeneous embedded systems [1284,1289,1290]. According to Wolfarm, cellular automata consist of many identical simple components, that together are capable of complex behavior [1291]. Alongside FPGAs, cellular automata has been used for cryptography [1292–1298], random number generation [1299–1302], systems modeling [1303–1312], and simulation [1313–1315]. Phase-Locked Loop (PLL) "synchronizes the frequency of the output signal generated by an oscillator with the frequency of a reference signal by means of the phase difference of the two signals" [1316]. In FPGAs the PLLs have been used for motor speed control [1317–1319], demodulator synchronization [1320–1322], and jitter detection [982, 1323–1327].

Ring oscillator in this list has the highest PDLY, with 52% of the documents published in the last three years. A ring oscillator is a cascaded combination of delay stages, connected in a close loop chain to generate an oscillating output [1328]. FPGAs' implementations of ring oscillators include physical unclonable functions [714, 717, 1329–1332], time to digital converters [1333–1337], and random number generators [984,1338–1347]. Other implementations techniques in FPGAs covered in this top are SVPWM (Space Vector Pulse Width Modulation) [1348–1354], LFSR (Linear-Feedback Shift Register) [1355–1360], FIFO (First-In First-Out) [1361–1369], RNS (Residue Number System) [1370–1373, 1373–1376], DMA (Direct Memory Access) [1377–1380], SIMD (Single Instruction Multiple Data Stream) [1381–1384], systolic arrays [1385–1389], and bloom filter [1235, 1390–1395].

2.3.13 Other applications

In this section, we present other FPGAs' applications not covered previously. Figure 2.28 shows the top other applications.

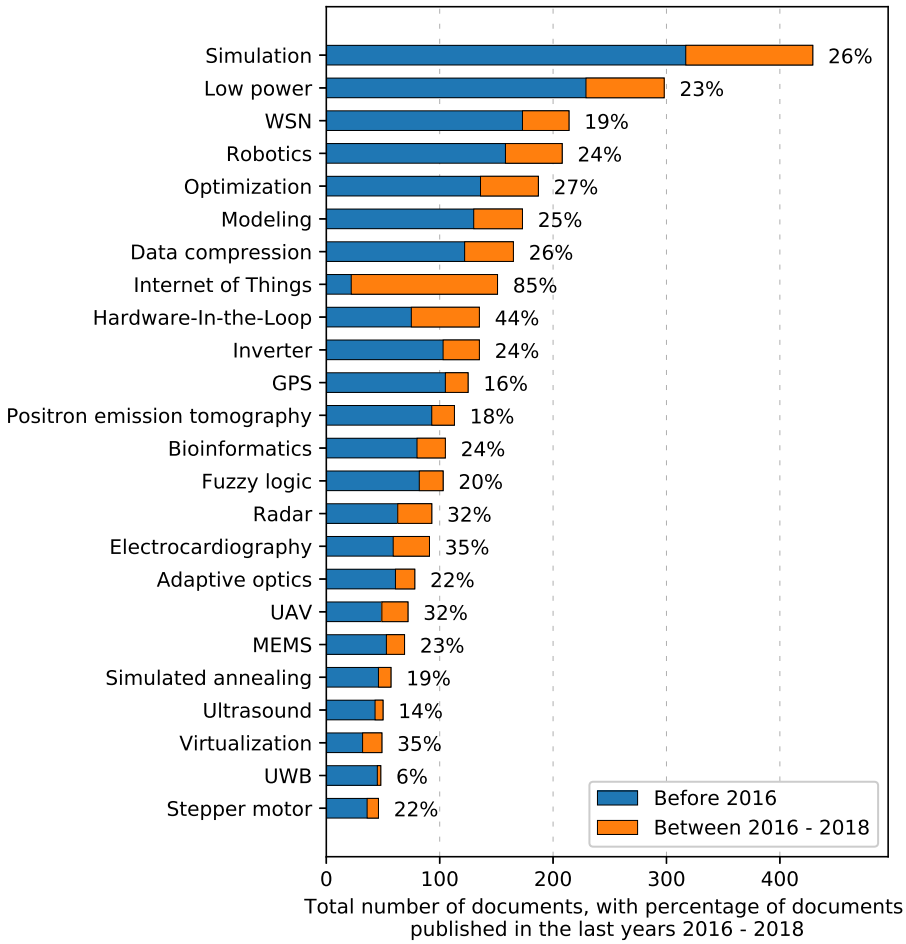


Figure 2.28: Other top applications in FPGAs' research

Simulation is the top one in this list, and it refers to an approximate imitation of the operation of a process or system [1396]. In this area, we found FPGAs' usage for the simulation of different systems, such as the described following:

- Power electronics [1397–1399, 1399–1431]
- Multiprocessors/multicore architectures [397, 1432–1436]
- Neural biological systems [1437–1440]
- Single even upsets (SEU) [1433, 1441–1444]
- Photovoltaic systems [852, 1445–1451, 1451–1453]
- Read-out detectors [1454–1456]

- Electrical machines [1457–1465],
- Distribution grids [1466–1472]
- Vehicles [1473–1478]
- BPSK and QPSK modulators [1479, 1480]
- Microprocessors cache [1481, 1482]
- Fuel cells [1483, 1484]
- Synthetic Aperture Radar (SAR) echo simulation [1485, 1486]
- Wind farms, turbines [1487, 1488]
- RFID tags [1489, 1490]
- Biochemical reaction [1491]
- MEMS (Microelectromechanical Systems) [1492]
- Nanoscale devices [1493]
- Quantum computers [1494]
- HPC (High-Performance Computing) power consumption [1495]

Low power applications are the second in this other applications list, which include low power applications for image processing [1496–1501], H.264 encoding [1144, 1146, 1502–1506], finite state machine [1279, 1507], memory design [1508–1510], and AES encryption [1511–1514]. The WSN (Wireless Sensor Networks) comprises wireless sensors that have a sensing comportment, on-board processing, communication, and storage capabilities to cooperatively monitor a large physical environments [1515]. FPGAs have been used in WSN for elliptic curve cryptography implementations in sensor nodes [1516–1521], energy efficient sensor nodes [1522–1524], ZigBee MAC layer functions realization [643, 1525], and ZigBee physical layer blocks simulation [1526]. Next, robotics applications (including mobile robots) in FPGAs involves:

- Localization [1527–1529, 1529–1533]
- Trajectory/path planing [873, 1534–1540]
- Visual servoing [858, 1541–1546]
- Navigation [389, 1531, 1547–1551]
- Stereo vision [1550, 1552–1555]
- Object/person follower/tracking [1545, 1556–1558]
- Ultrasonic sensors [1559–1563]
- Robot Operating System (ROS) [1531, 1564–1567]

- Educational [1568–1570]
- Motion control [1571–1573]
- Vector rotation [1561, 1574, 1575]
- Obstacle avoidance [1576–1578]
- Arm robot joints control [1579, 1580]
- Mapping [1581]
- Collaborative robotics [1582]
- Spatial cognition [1583]
- Velocity estimation [1584]

Optimization applications in FPGAs enclose power optimization [1585–1587], CRC (Cyclic Redundancy Check) look-up table [1588], pipelines [1589, 1590], Particle Swarm Optimization (PSO) [1591–1593], SM3 hash algorithm [1594], FIFO stack [1595], matrix multiplication [1596], torque ripple [1597], memory usage [1598], banking model [1599], and thermoelectric coolers [1600]. Modeling is the use of mathematical models as an idealization of a real-world phenomenon, for predicting the value of a variable at some time in the future [1601]. Similarly to simulation, FPGAs have been used in several modeling applications:

- Control systems [1602–1606]
- Power electronics [1404, 1462, 1607–1610]
- Network on chip [1611, 1612]
- Thermomechanical systems [1613, 1614]
- Employees behavior and interactions in workplace [1303]
- Computer networks [1615, 1616]
- Arousal content [1617]
- FIFO stack [1595]
- HPC power consumption [1495]
- Meteorological systems [1618]
- UAV (Unmanned Aerial Vehicle), vehicles, and mobile robots [1619, 1620]
- Renewable energy systems [1603, 1621, 1622]
- RF (Radio Frequency) power amplifier [1623]
- Urban traffic [1312]

Data compression is a reduction in the number of bits needed to represent the data [1624]. In FPGAs data compression has been implemented in the LZ77 algorithm [1625–1628], Huffman coding [1629–1631], LZW (Lempel–Ziv–Welch) algorithm [1626, 1632–1635], and hardware accelerator compressing techniques [1625, 1627, 1636–1639]. Internet of Things (IoT) connects billions of devices to the Internet, devices that combine sensing, computation, and communication techniques to deliver remote data collection and system control [51]. IoT in this list is the application with the highest PDLY, with 85% of the documents published in the last three years. For IoT applications, FPGAs have been used in improving devices security [1640–1642], data encryption [835,1521,1643–1645], edge computing [1646–1648], FPGA-based gateways [1649,1650], and fog computing platforms [1651, 1652].

Finally other FPGAs applications in this list includes Hardware-In-the-Loop (HIL) [1492, 1653–1660], GPS (Global Positioning System) [1661–1676], Positron Emission Tomography (PET) [1677–1702], bioinformatics [1703–1720], fuzzy logic [1721–1731], radar [1033, 1732–1741], Electrocardiography [1742–1759], adaptive optics [1760–1772], Unmanned aerial vehicles [871, 1773–1780], MEMS [551, 551, 1781–1789], simulated annealing [1790–1798], ultrasound [1799–1810], virtualization [1811–1816], UWB (Ultra-wideband) [1529, 1817–1822], and stepper motor applications [1823–1840].

2.3.14 Applications mapping

In this section, we describe the co-occurrence mapping for the different FPGAs' applications. Hence, we generated a co-occurrence network mapping of the 35 most relevant applications from the dataset pre-processed output generated by ScientoPy. Then, we used VOSviewer [1841] for the network map formation. Figure 2.29 shows this co-occurrence network map. Here we find 5 clusters that are described as follows. The yellow cluster indicates applications related to signal to process. The purple cluster is related to the applications that are related to low power implementations. Then, the green cluster contains applications related to security implementations. Next, the blue cluster is related to high-performance and high-reliability systems. Finally, the red cluster is related to real-time applications.

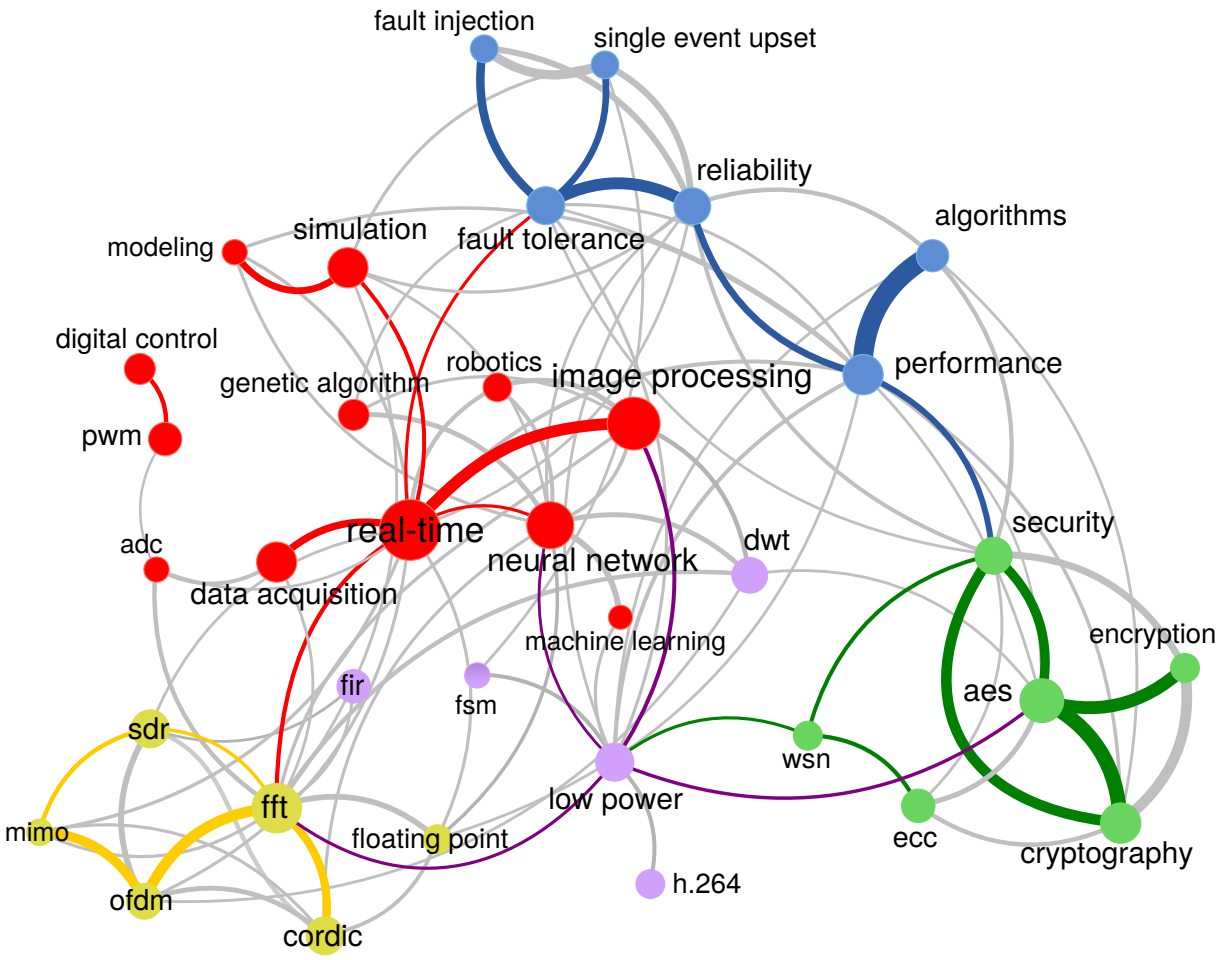


Figure 2.29: Co-occurrence network mapping of author keywords related to FPGAs' applications. Colors represent groups of applications that are relatively strongly linked to each other. The size of the node signifies the number of documents related, and the width of the lines represent the strength of the relationship between two nodes.

For the signal processing cluster (yellow color) we find relations that indicates for intance that MIMO is supported by OFDM [523, 525, 1842–1844], and OFDM is supported by FFT implementations [913, 915, 1845, 1846]. The FFT implementations are supported by CORDIC [906–909], and also are designed as low power implementations [907, 1847]. For the security cluster (green color), we found that AES has an strong relationship with security, encryption, cryptography, and also with low power implementations [845, 1511]. Similarly, we found that FPGAs' implementations have helped to add security to WSN nodes [1516–1518], and low power processing capabilities [1848–1850].

In the red cluster, we find FPGAs' applications focused in real-time implementations, such as data acquisition [940, 1851–1853], simulations [1397, 1400, 1457, 1854], neural networks [1855–1857], and image processing [1858–1865]. Finally, the blue cluster shows that the fault tolerance and high reliability systems are based in fault injection impelmentations [1866, 1867] and single event upset tolerance mechanisms [1868–1870]. In addition, other relevant relations are shown in colored lines, like digital control with PWM [1871, 1872], simulation with modeling [1432, 1495,

1873], and performance with algorithms [1874–1876].

2.4 Graphic processing units

GPUs are built as a scalable array of Streaming MultiProcessors (SM). The hardware parallelism of the GPU is achieved by replicating this architectural building block (see Figure 2.30). Each SM in a GPU is designed to support the concurrent execution of hundreds of threads. There are generally multiple SMs per GPU, so it is possible to have thousands of threads running simultaneously on a single GPU [1877].

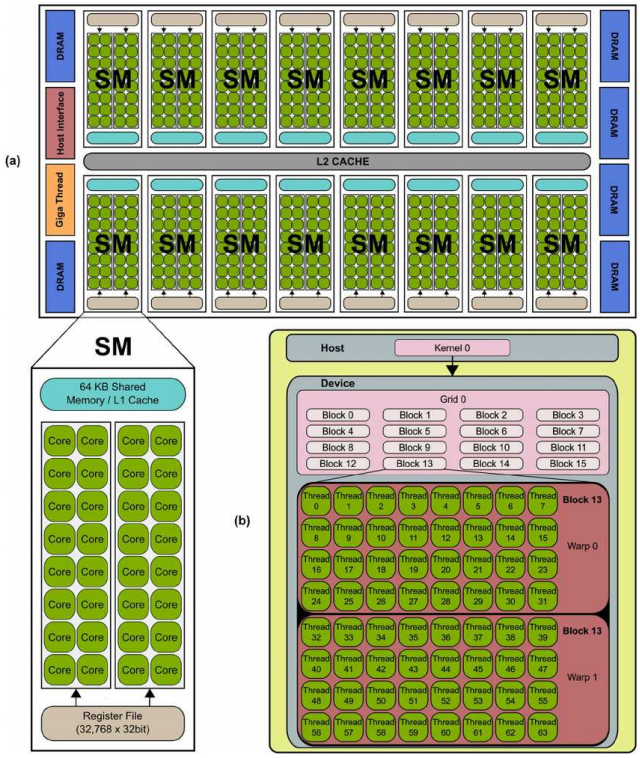


Figure 2.30: Typical architecture of an NVIDIA GPU. The GPU consists of a set of Streaming MultiProcessors (SM). Each SM consists of several Flow Processor (SP) cores, as shown for the NVIDIA Fermi architecture (a). The programmer controls the resources of the GPU through the CUDA programming model, shown in (b). [1878]

2.4.1 GPUs' applications

Using a bibliometric dataset from Scopus and WoS obtained with the search string "GPU*" OR "Graphic processing unit*", the most important applications related to authors' keywords were found, see Figure 2.31. Machine learning technies are the most popular for GPUs in this dataset, with convolutional neural networks implementations [1879–1882], genetic algorithms [1883–1885], Adaboost [1886], and others. Also, GPUs have been widely used for image processing using different frameworks and programming languages such as Caffe [1887], OpenVINO [1888], OpenCL [1889], or CUDA [1890]. These image processing applications include image segmentation [1891], tomographic image reconstruction [1892–1894], and optical flow [1895].

Rendering applications include accelerated volume rendering [1896–1898], illumination tech-

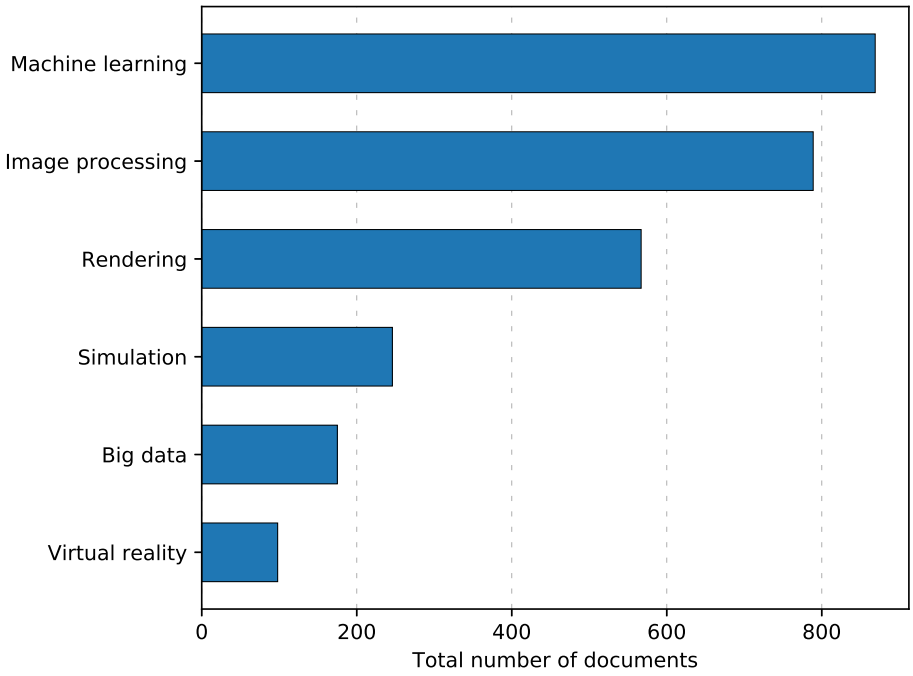


Figure 2.31: Top GPUs' applications, and the number of documents found in Scopus and WoS related to them.

niques [1898–1900], ambient occlusion [1901], among others. Simulation applications are described in deep in the next sub section. Finally other applications includes big data [1902–1906] and virtual reality [1907–1910].

2.4.2 GPU-based simulations

Figure 2.32 shows the top GPU-based simulations implementations. These include the simulation of fluids [1911–1914], molecular dynamics [1915–1919], crowds movement [1920–1926], surgical procedures [1927–1931], cloth dynamics [1932–1934], circuits [1935–1938], particles [1939–1942], traffic [1943–1950], and electrical power systems [1951–1954].

For traffic simulation specifically, we found only one document focused on public transport simulations [1948]. In this study, a mesoscopic, multi-modal, queue-based mobility simulator is implemented on a GPU, including a detailed public transit model.

2.4.3 Architecture

The architecture of the GPUs is dynamic and evolves over the years. For example, in the last 10 years, NVIDIA has removed 6 different types of architectures, from Tesla in 2008 to Volta in 2018. However, the common size for these architectures has been their small cache memory size compared to CPUs. For example, the largest size of L1 cache memory in a GPU only reaches 64KB.

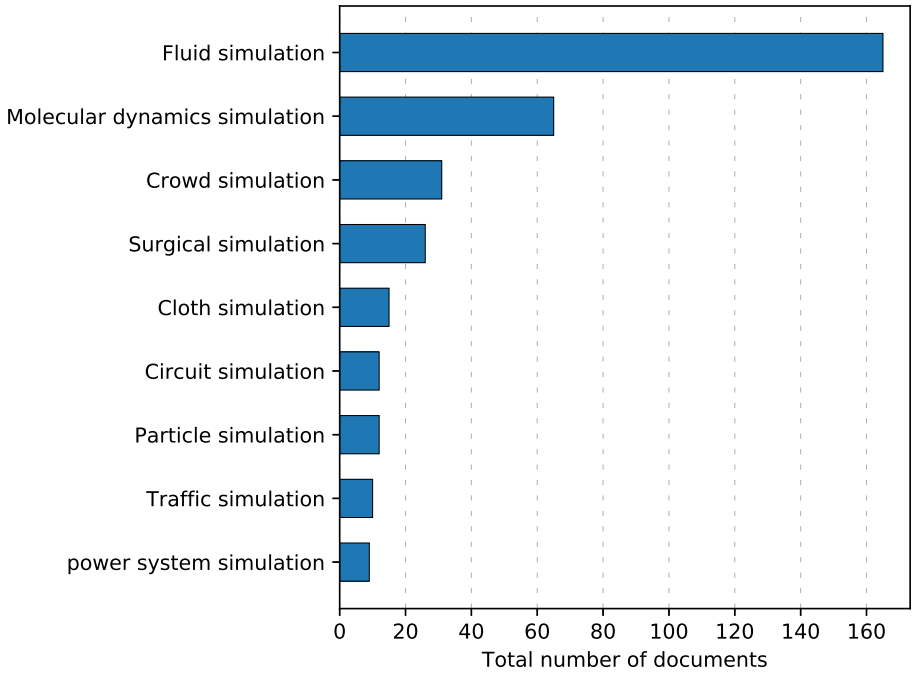


Figure 2.32: GPU-based simulations, and the number of documents found in Scopus and WoS related to them.

2.5 Multi-core

A multi-core processor is an integrated circuit with two or more separate processing units, called cores, each of which reads and executes program instructions as if the computer had multiple processors [1955]. Modern CPUs have multiple levels of CPU caches. The first CPUs that used a cache had only one level of cache; unlike subsequent level 1 cache, it was not divided into L1d (for data) and L1i (for instructions). Almost all current CPUs with caches have a split L1 cache. They also have L2 caches and, for larger processors, also L3 caches. The L2 cache is generally not divided and acts as a common repository for the already divided L1 cache. Each core of a multi-core processor has a dedicated L2 cache and is generally not shared between the cores. The L3 cache and the higher level cache are shared between the cores and are not split [1956]. Today advanced processors such as Intel Xeon Gold have up to 1.25MB of L1 [1957] cache.

There are currently different types of multi-core systems offered by Intel and AMD. Some are described below.

- Intel Core i7-8550U, 4 cores, 8 threads, L1 256 KB cache, L2 1MB, L3 8MB
- Intel Xeon Gold 6210U, 20 cores, 40 threads, cache L1 1.25 MB, L2 20MB, L3 27.5MB
- Intel Xeon Phi 7295, 72 cores, 288 threads, cache L1 4.5 MB, L2 36MB
- AMD Ryzen 9 3950X, 16 cores, 32 threads, cache L1 1 MB, L2 9MB, L3 64MB

2.5.1 Multi-core's applications

Using a bibliometric dataset from Scopus and WoS obtained with the search string "multi-core" OR "multi core", the most important applications related to authors' keywords were found, see Figure 2.33. Here we find machine learning classifiers [1958, 1959], and genetic algorithms [1884, 1960–1963]. Secondly, we find simulation applications which are described in deep in the next sub section. Next we have cloud computing [1964–1968], big data [1969–1974], image processing [1975–1981], data mining [1982–1984], systems modeling [1985–1987], Digital Signal Processing (DSP) [1988–1996], and molecular dynamics [1997–2001].

2.5.2 Multi-core-based simulations

In this section we describe the simulation applications based in multi-core systems. Figure 2.34 shows these top simulations applications, that includes circuit simulation [2002, 2003], molecular dynamics [2004–2006], power systems [2007, 2008], biomolecular [2009–2011], reservoirs [2012–2014], traffic [2015–2019], crowds [2020, 2021], plasma [2022], lithography [2023], and social behaviors [2024, 2025].

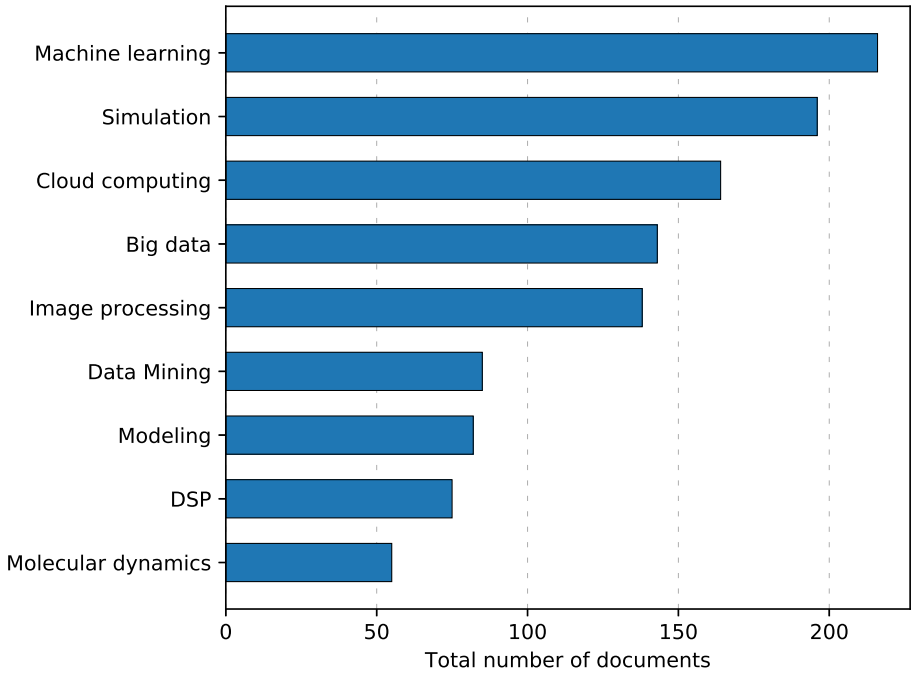


Figure 2.33: Top multi-core's applications, and the number of documents found in Scopus and WoS related to them.

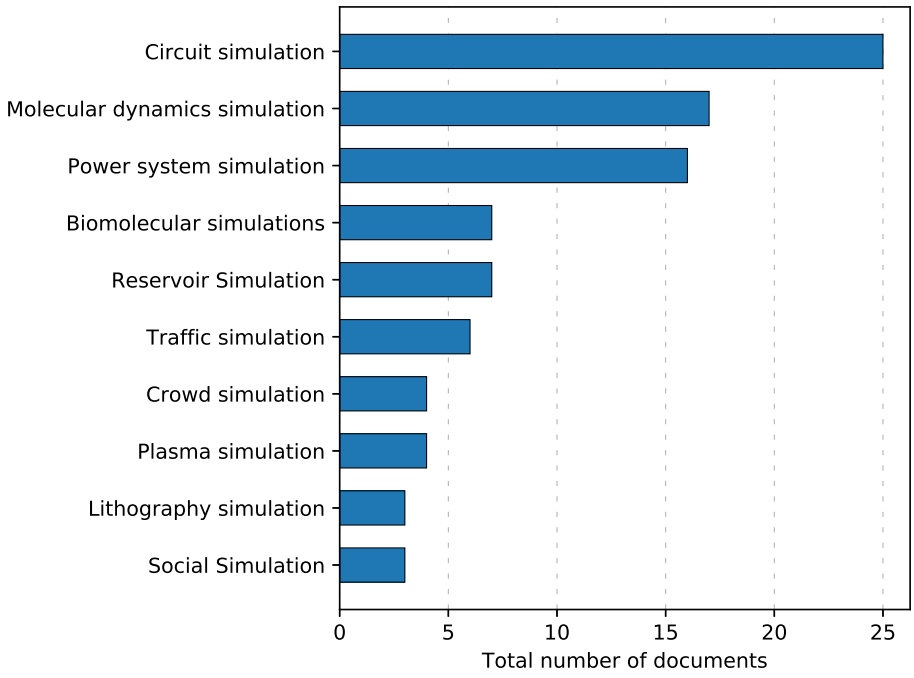


Figure 2.34: Top simulation implementations using multi-core with the number of documents found in Scopus and WoS related to them.

2.6 Discussion

A new scientometric open-source tool called ScientoPy was developed to facilitate the state-of-the-art's construction. ScientoPy can perform data analysis by extracting the top topics of a selected criterion, such as top authors, top countries, top institutions, top author's keywords, and others. Besides, it can plot the data analysis results in four different ways: timeline graph, bar graph, evolution graph, and word cloud. Additionally, we can perform in ScientoPy another type of data analysis, such as trending topics, specific topic searches, and wildcard searches. With these capabilities, we can find several results from a bibliographic database, like first top author's evolution, countries or institutions evolution and participation over time, institutions participation of a selected country, and specific topic or trending topics evolution based on author's keywords.

To get the background of IoT development, a scientometrics review was performed about it over a data set of 19,035 documents published during a period of 15 years (2002–2016) from two databases (Clarivate Web of Science and Scopus) using ScientoPy. Analysis by country affiliation of the primary author shows a major increase in the number of publications for IoT in countries where the government has possibly implemented policies that improve the development of IoT. From 2014 to 2016, there was a sharp growth of smart environments, including smart city, home, grids, and other surfaces with technology incorporating Big Data and cloud computing into IoT devices. Inside smart city we found that transportation (ITS, smart transportation, and smart mobility) applications have a strong relationship with big data [228–231] and simulation [232–234], generating the bases for public transport simulation.

Security [163–165] and privacy [175,178,179] are major concerns for many applications such as smart home and grid. Top trending topics demonstrate that cloud integration with IoT devices is enabling the implementation of smart environments. Nevertheless, security and privacy in these environments are important growing concerns for IoT researchers and industry. WSNs are one of the most utilized technologies enabling the IoT. Furthermore, Fog computing has emerged as a promising edge device to decentralize data processing, decrease latency, and bring more reliability for WSN in IoT. Likewise, research on Software Defined Networks (SDN) grew rapidly during the last year, offering more efficient nodes, mobility, resources management, and improved security of IoT networks. The related trending topics offer unique opportunities for IoT innovations and start-ups in pursuit of an efficient, secure, and reliable IoT environment.

A review of the three main parallel processing architectures was performed, including Field-programmable gate array (FPGA), Graphics Processing Units (GPU), and multi-core processors. These reviews were directed in the applications developed in these architectures and focusing in applications related to simulation in public transport systems.

Inside FPGAs we found a wide range of applications, from real-time data processing to neural network implementations. In this review we divided these applications into eleven categories, and in each category we presented the applications with most documents related to them, totaling 150 applications described here. These applications were divided in digital signal processing [380–382], image processing [383–385], cryptography [386–388], parallel processing [389, 390], fault tolerance systems [391–393], low power systems [394, 395], simulation [396–398], digital control [399–401], artificial inteligence [402–404], networking [405, 406], and big data [407–410].

For GPUs we found applications related to machine learning [1879–1886], image processing [1891–1894], rendering [1896–1898], simulation [1911–1954], big data [1902–1906], and virtual

reality [1907–1910]. Likewise, for multi-core applications we found machine learning [1884, 1958–1963], simulation [2002–2018, 2020–2025], cloud computing [1964–1968], big data [1969–1974], image processing [1975–1981], data mining [1982–1984], systems modeling [1985–1987], DSP [1988–1996], and molecular dynamics [1997–2001].

Table 2.14 summarizes the documents related to parallel simulation applications for traffic and transit systems. For the FPGA's parallel architecture, we found only one document specific to urban traffic simulation. Here the authors in 2005 developed a microscopic simulation of the road traffic. They simulated the Portland road network with 124,000 road segments and 100,000 intersections, achieving a speedup factor of 4.5 [1312]. For GPU's parallel architecture, we found 5 implementations, where 4 are related to road traffic and one to public transit simulation. In 2012 Wang et al. built a GPU Based traffic parallel simulation module, which was able to simulate three hours (10800 seconds) road traffic of a 40×40 lattice road network, with 5000 vehicle agents in 109 seconds, achieving a speedup of 105 and a real-time factor of 102 [1943]. Later, in 2014, Xu et al. implemented a mesoscopic road traffic simulation on CPU/GPU. This implementation was tested in a road network of 10,201 nodes, 20,100 unidirectional links, and 100,000 vehicles during 1000 simulation ticks (each tick is 1 second). The simulation time for this network was 4720 ms for CPU and 423 ms for GPU, getting a speedup of 11.2 and a real-time factor of 2364 [1945].

Table 2.14: Documents related to traffic and transit parallel simulation

Document Title	Year	Parallel architecture	Model type	Simulation core	Speedup factor	Real time factor	Simulation complexity	Reference
Urban traffic simulation modeling for reconfigurable hardware	2005	FPGA	Microscopic	Road traffic	4.50	Not specified	100,000 intersections	[1312]
A GPU based traffic parallel simulation module of artificial transportation systems	2012	GPU	Microscopic	Road traffic	105.00	102.00	1600 intersections and 5000 vehicles	[1943]
Mesoscopic Traffic Simulation on CPU/GPU	2014	GPU	Mesoscopic	Road traffic	11.20	2364.00	10,201 nodes and 100,000 vehicles	[1945]
Supporting real-world network-oriented mesoscopic traffic simulation on GPU	2017	GPU	Mesoscopic	Road traffic	2.37	1897.00	4106 OD pairs, 100,000 vehicles	[1944]
GEMSim: A GPU-accelerated multi-modal mobility simulator for large-scale scenarios	2019	GPU	Mesoscopic	Public transit system	Not specified	1300.00	27,873 stops and 100,000 passengers	[1948]
A Framework for Mesoscopic Traffic Simulation in GPU	2019	GPU	Mesoscopic	Road traffic	5.00	Not specified	4103 OD pairs, 300,000 vehicles	[1950]
Distributed-Parallel Road Traffic Simulator for Clusters of Multi-core Computers	2012	Multi-core	Microscopic	Road traffic	3.32	163.00	1024 Crossroads	[2015]
Real-time Traffic Information System Using Microscopic Traffic Simulation	2013	Multi-core	Microscopic	Road traffic	Not specified	60.00	1,300 cross-sections and 120,000 vehicles	[2016]
Parallel Microscopic Simulation of Metropolitan-scale Traffic	2013	Multi-core	Microscopic	Road traffic	16.00	0.86	145,665 roads, 4,349,130 vehicles, and 0.1s step time	[2017]

In 2017 Song et al. implemented the mesoscopic traffic simulation on GPU developed in [1945] to a real-world scenario. The scenario was the Singapore expressway system, which is made up of 3179 nodes, 3388 links, and 9419 lanes with a demand modeled as trips from 4106 origin-destination (OD) pairs. There were simulated in total 100,000 vehicles loaded into the peak traffic scenario during 1000 simulation ticks (each tick is 1 s) the execution time of this simulation was 1250ms for CPU against 527 ms for GPU, getting a speed up 2.37 and a real-time factor of 1897 [1944].

Next, in 2019, Saprykin et al. developed GEMSim, a GPU-accelerated multi-modal mobility simulator for large-scale scenarios. This is a mesoscopic multi-modal, queue-based mobility simulator for public transit systems. Here the large-scale scenario of Switzerland with 513,770 nodes and 1,127,775 road links, 27,873 stops, and 21,847 routes was simulated. The simulation ran for a full day (86400 seconds), and the execution time was 290 seconds, equivalent to a real-time ratio of 298 for a population of 5.2 million, and a real-time ratio of 1300 for 100,000 population size [1948]. The same year, Vinh and Tan created a framework for mesoscopic traffic simulation in GPU tested in an updated Singapore Expressways network, which has 3186 nodes, 3386 links, and 9437 lanes, with a demand modeled as trips from 4103 origin-destination pairs. There were simulated up to 300,000 vehicles, getting a speed up of 5 times against the CPU [1950].

For multi-core parallel architecture, first in 2012 Potuzak developed a distributed-parallel road traffic simulator for clusters of multi-core computers, tested in regular square grids of 64,256, and 1024 crossroads. The simulations ran for 1 hour (3600 seconds) with no number of vehicles specified with an execution time for the best cases of 22 seconds for 64 crossroads (real-time factor: 163), 86 seconds for 256 crossroads (real-time factor: 41), and 245 seconds for 1024 crossroads (real-time factor: 14) [2015]. Then in 2013, Bruegmann et al. developed an online, real-time traffic information system called OLSIMv4, which uses microscopic traffic simulations exploiting the thread-level parallelism on multi-core machines using a coarse-grained parallel microscopic simulation model. This simulation runs in the highway network of North Rhine-Westphalia (NRW), Germany. The simulated network contains more than 3,000 loop detectors bundled into 1,300 measurement cross-sections with an average statistical distance of 3.5 Km. The simulation ran for 60 minutes with 120,000 vehicles with an execution time 60 seconds, resulting in a real-time factor of 60 [2016].

Finally, the same year, Fernandes et al. developed a parallel microscopic simulator capable of simulating metropolitan-scale traffic using OpenMP. For the simulation they used a real-world road network of San Francisco Bay Area which comprises 145,665 roads with a total of 27,439 Km. The simulation runs in 60 seconds intervals with a step time of 0.1 seconds, and generating a vehicle in each road every 2 seconds following a negative exponential distribution, totaling 4,349,130 vehicles. Whit these parameters, they achieved an execution time of 70 seconds (real-time factor 0.86), and a speedup factor of 16 times, using 24 processors against the single processor simulation [2017].

Chapter 3

Public transport routes simulation

In this chapter, we describe the behavior and main components of the public transport systems. Then, we discuss the existing techniques for public transport traffic simulation.

3.1 Public transport system

In a public transport system, the buses, trains, or other forms of transport are used by people to travel from one place to another [2026]. Figure 3.1 shows a small public transport system example, which consists of three stops (S_i) separated 2 km and two routes (R_1 and R_2). In this system, we have, for instance, passengers from the origin stop S_1 that travel to the destination stops S_2 and S_3. The origin-destination matrix (OD) denoted as D represents the number of passengers that travel from each stop to another. For example, if we have 10 passengers that travel from S_1 to S_2, the value $D_{1,2}$ is 10.

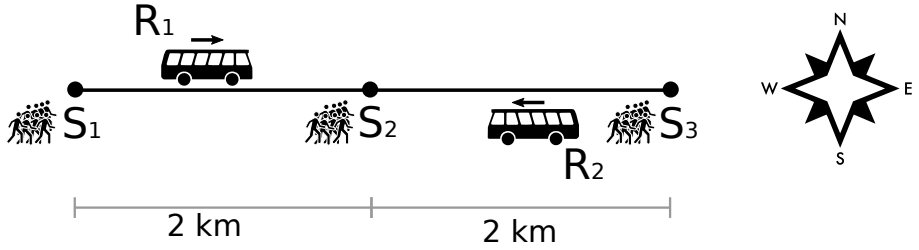


Figure 3.1: Small example of a public transport systems with three stops and two routes.

In this way, the OD matrix can describe the full system demand, as shown in Equation (3.1). Here, we see a diagonal of zero, which indicates that there are no passengers that travel from the origin station to the same origin station.

$$D = \begin{bmatrix} 0 & 10 & 20 \\ 10 & 0 & 10 \\ 20 & 10 & 0 \end{bmatrix} \tag{3.1}$$

The routes are designed to transport passengers from one stop to another. Figure 3.1 shows two routes (R_1 and R_2). R_1 has the direction west to east, and R_2 has the direction east to

west. The RT_r value defines the total trip time (in seconds) for route r, that is the time needed by the bus to complete the full route. The value f_r defines the frequency (in seconds^{-1}) of the route r, and it represents how often the bus is dispatched for each route. Therefore, the number of buses needed for each route is defined by Equation (3.2) as BR_r, where the symbols "⌈" and "⌉" represent a ceiling function that returns the nearest integer that is greater.

$$BR_r = \lceil RT_r f_r \rceil \tag{3.2}$$

For instance, we need an R_1 frequency of 5 min ($f_r = 1/300$ s^{-1}), and the total trip is 570 s, defined by Equation (3.3), where N is the number of stops:

$$\begin{aligned} RT_1 &= \frac{\text{Total distance}}{\text{Bus avg. speed}} + (\text{Stop time}) \times N \\ RT_1 &= \frac{4 \text{ km}}{30 \text{ km/h}} + (30 \text{ s}) \times 3 \\ RT_1 &= 570 \text{ s} \end{aligned} \tag{3.3}$$

As a result, the number of buses needed for R_1 for this case is defined by Equation (3.4) as:

$$\begin{aligned} BR_r &= \lceil 570 \text{ s} \times \frac{1}{300 \text{ s}} \rceil \\ BR_r &= 2 \end{aligned} \tag{3.4}$$

As we can see in Equation (3.2), if we increase the frequency of a route, we will need to have more buses to meet the demand. Nevertheless, the number of buses is limited by the total fleet size or even by the roads' capacity. Then, to find the route's frequency, we have an optimization problem described by Equation (3.5), where the objective is to minimize the total travel time, restricted by the total fleet size [2027].

$$\begin{aligned} &\text{minimize} \sum_{i \in N} \sum_{j \in N} D_{ij} T_{ij}(\mathbf{f}) \\ &\text{subject to:} \sum_{r \in R} \lceil RT_r f_r \rceil \leq \text{total fleet size} \end{aligned} \tag{3.5}$$

where:
N = total stops;
R = total routes;
D_{ij} = OD (Origin-Destination) demand;
T_{ij} = passenger travel time;
RT_r = round-trip time on route r;
f_r = frequency on route r;

The passenger travel time T_{ij} includes the expected waiting time, as a function of the routes' frequencies $\mathbf{f}$. Unfortunately, this travel time cannot be calculated directly, because it depends on other variables such as the buses' capacity, the stops' capacity, and the routes' stops' table. Furthermore, the buses' free seats depend on the buses' capacity and the number of passengers that have boarded the buses at the previous stops. This correlation between the buses' free seats with other variables of the systems converts this into an NP-hard problem, where the approach to this problem relies on heuristic techniques for systems of a reasonable size [2027].

3.1.1 Passenger demand in public transport systems

The origin-destination matrices (OD) specifies the passengers' travel demands between the origin and destination nodes in the network. Geographic information systems (GIS) have been used effectively for OD data analysis, supporting geocoding OD survey data to point locations [2028]. Figure 3.2 shows an arbitrary OD matrix for one of the oldest trunks of Transmilenio BRT, in Bogotá, Colombia, displayed as a bubble chart. Each entry in the matrix indicates the estimated demand of trips originating in the stop located at the corresponding x-coordinate and finishing at the stop in the corresponding y-coordinate (southbound trips, lower diagonal section in orange) or vice-versa (northbound trips, an upper diagonal matrix in red). The diameter of the bubble is proportional to the current demand. This OD matrix indicates with the diameter of the bubble the current demand, where nine stops on this trunk line are most demanded (Portal Norte, Alcala, Calle 100, Calle 76, Calle 72, Calle 63, Marly, Calle 45, Av. Jimenez).

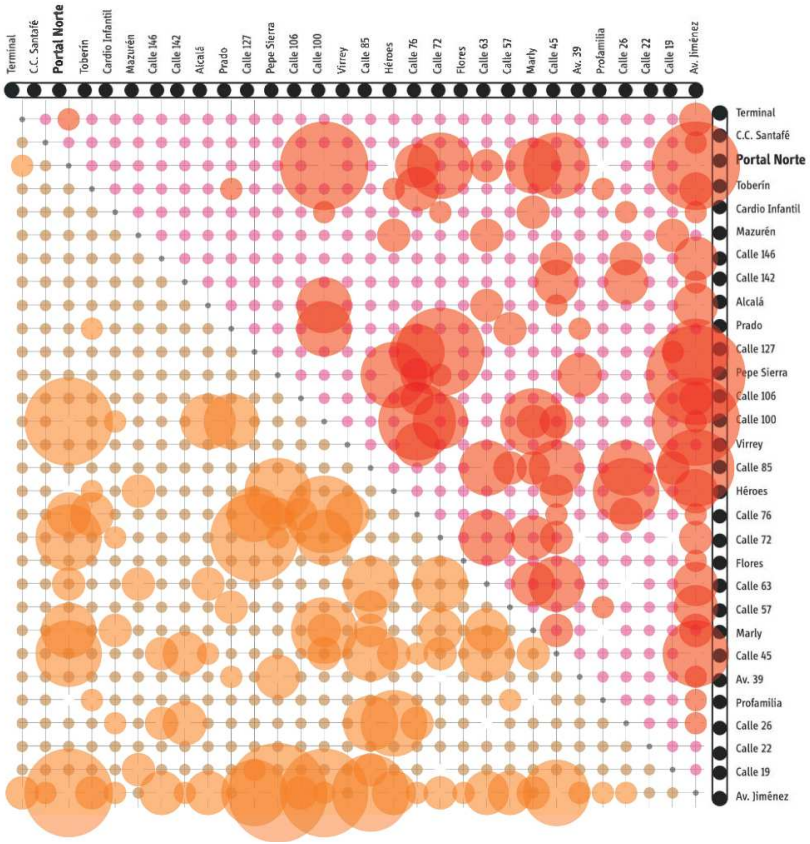


Figure 3.2: Origin-Destination matrix example. [2029]

The OD matrix is dynamic because it is time-varying. Inside a city's public transport system, the OD matrix varies in weekdays and weekends, and even between different hours of the day. A high-quality OD matrix is a fundamental prerequisite for any serious transport system analysis. Surveys have been used to define the OD matrices [2028, 2030], nevertheless more sophisticated methods are used today for this purpose, such as passive smartcard fare collection system data [2031, 2032], or mobile network data [2033].

3.1.2 Public transport vehicles routes

In public transport systems, the vehicles (trains or buses) follow a route to meet the passengers' demand. The route is defined by a set of stops, where the bus picks up or alights passengers. Also, the route's frequency is defined as how often the bus is dispatched for each route. That also means how frequent a bus route passes in one stop. Figure 3.3 shows the stop table for 4 different routes. The first one (down to up), is an all-stops route, that means that this route stops in all the stations. The other three routes are express routes, which stop in the circled red stations. The express routes are designed to meet the demand of the highest origin-destinations combinations.

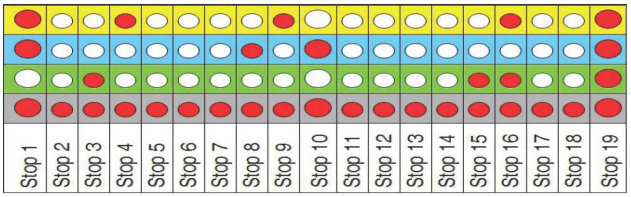


Figure 3.3: Stops table example for the buses' routes. Red circles indicate the stopping station on the corresponding route. [2029]

Due to the dynamic nature of the OD, one of the most important components in determining the public transport service is the selection of the most suitable route's frequency by time-of-day and day-of-week. The routes design also includes the developing of timetables, scheduling buses, and scheduling drivers. The route layout design depends on the passenger flow. Due routes are configured to provide a direct or indirect connection between origin-destination demand for passengers.

3.2 Simulation models and software

The public transport systems handle a huge quantity of passengers (up to millions), buses, and routes per day, making this high complexity system. There is much literature focused on the simulation and optimization of the different variables of these systems. Table 3.1 describes the different simulation models applied to this system's variables. In the literature, the most relevant topics for public transport simulation are traffic (10 articles), route programming or scheduling (5 articles), economic aspects (4 articles), and route design (3 articles). Microscopic models are the most used for the simulation of these variables.

Within the simulation of the behavior of the routes, some studies cited in Table 3.1 limit the size of the problem, so that the simulation can be performed in conventional computing architectures. For example, Ceder, simulates new strategies for routes, using only 10 routes [2047]. Next, Zhang creates an artificial urban transit system (AUTS) to solve the problem of passenger assignment, where he concludes that the scale of the problem handled by this system should be limited, since as the number of passengers increases in the system, the simulation time of the AUTS increases rapidly, taking up to 10 days to solve the complete problem [26].

Hadas develops an optimal coordinator for the transit of public transport vehicles using operational tactics based on simulation. To accomplish this objective, he uses a model based on Dynamic Programming (DP), in which a complex problem is solved by dividing it into a

Table 3.1: Simulation traffic models for public transport

Simulated component	Simulation model	References
Bus layout	agent-based	[2034, 2035]
Bus-networks	agent-based	[2036]
Demand	agent-based	[15–17]
	multinominal	[2037]
Diseases	agent-based	[2038]
Dynamics	MBS	[2039]
Economy	activiy-based	[2040]
	agent-based	[2041, 2042]
	Demand-model	[2043]
Passenger decision	agent-based	[18]
	experimental simulation	[2044]
Quality	System-dynamics	[2045]
Reliability	microscopic	[2046]
Routes	agent-based	[26]
	event-oriented	[2047]
	microscopic	[2048]
Scheduling	Dynamic-programming	[28]
	mesosopic	[29]
	microscopic	[32]
	own model	[30]
	stochastic	[31]
Stations design	petri nets	[2049]
Traffic	agent-based	[2050]
	microscopic	[19–22] [23–25]
	SMITE	[2051]
	State-space	[2052]

collection of simpler subproblems [30]. Unfortunately, this type of division can lead to the simulation delivering data that allows only local and non-global optimizations to be reached.

3.2.1 Traffic simulation software

There is much literature that deals with topics about the simulation of traffic networks especially focused on traffic simulation in private vehicles [7, 9, 11, 12, 33–37]. This literature presents simulation systems based on the different models already explained (macroscopic, microscopic, and mesoscopic). With the help of these models, different computational tools have been designed to help simulate traffic environments. For macroscopic models there are for example tools such as: Strada [10], Metacor [2053], Visum [2054], Emme [2055], among others. On the other hand, SUMO [2056], PTV VISSIM [2057] and Aimsun [2058] are some of the tools available that allow traffic simulation with microscopic models. For mixed or mesoscopic models some of the existing tools are: OmniTRANS [2059], TransModeler [2060] and the Aimsun [2058].

For public transport systems, in Bogotá, Colombia, the BRT system Transmilenio uses two of the most recognized tools for strategic route planning. These tools are PVT Vissim for microsimulation (traffic simulation at intersections, stop crowds simulation, etc.) and Emme for route planning (macrosimulation). With the PVT Vissim it is possible to carry out the specific traffic congestion simulation at an intersection, a traffic light crossing or lane sections, without

these unit simulations interacting with each other to predict a global behavior. On the contrary, Emme allows planning routes based on predictions of passenger demand.

Optimizing the routes' frequencies has been widely studied because this type of optimization can reduce the operating costs and travel times of passengers [2061–2063]. Unfortunately, frequency programming optimization for buses and public transport trains is known as a class of NP-hard [2064] problems, which cannot be solved in polynomial time [2065], which indicates than an algorithm may take an indeterminate time to find the solution to this problem. For this reason, different studies have proposed various reduction and heuristic methods and algorithms to address the complexity of NP-hard problems in public transport systems [2066–2089].

3.3 Traffic simulation parameters specification

For this research work, we define the public transport system parameters' specification with the following conditions and variables. First, we have the system conditions that are defined in Table 3.2. These conditions define the total number of stops, a full OD matrix of size $N \times N$, the max passenger capacity of each stop, and the stop position.

Table 3.2: System conditions' definitions and symbols.

Variable Name	**Symbol**
Total number of stops	N
Origin-destination matrix	**OD**
OD value for stop i to j	D_{ij}
Stops max capacity	SC_n
Stops X position	SPX_n
Stops Y position	SPY_n

On the other hand, Table 3.3 defines the variables related to the routes and buses. Here, we find the total number of routes, the maximum number of buses available per route, the frequency of each route, the maximum passenger bus capacity, and the route stops' table array. The stops' table array represents the stations (or transit stops) where the bus route stops.

Table 3.3: Routes variables' definitions and symbols.

Variable Name	**Symbol**
Total number of routes	R
Max buses per routes	BR_r
Routes frequency	f_r
Max bus capacity	BC
Route stop table array	$stops\_table_r$

Next, Table 3.4 presents the simulation output variables, which indicate the performance of the public transport system with the actual routes' configuration. These output variables consist of the total departed passengers per stop, the alighted passengers at the destination stop, the

total average passengers' commute time, and the average passengers' commute time for the alight stop.

Table 3.4: Simulation output variables' definitions and symbols.

Variable Name	Symbol
Departed passengers from stop	DPS_n
Alighted passengers at stop	APS_n
Average passengers commute time	ACT
ACT at alight stop n	$ACTS_n$

3.4 Simulation performance indicators

Table 3.5 shows the simulation performance variables. These variables indicate the simulation execution time and how fast the parallel simulation is relative to the real system and the sequential execution.

Table 3.5: Simulation performance variables' definitions and symbols.

Variable Name	Symbol
Total simulation time	tst
Total parallel simulation execution time	pst
Total sequential simulation execution time	sst
Real-time factor	rtf
Speed-up factor	suf
Efficiency	ef
Number of processing threads	p

Simulation performance can be measured using two measures of effectiveness, namely the real-time factor and the speed-up factor. The real-time factor is a measure of the relative speed of simulation concerning real time [43]. In this work, we measure the real time factor of the parallel implementation by using Equation (3.6). For example, if we are simulating 1 h (3600 s) of the public transport systems' routes in 3 s of execution time by the parallel model, the real-time factor will be 1200.

$$rtf = \frac{tst}{pst} \tag{3.6}$$

On the other hand, the speed-up factor (suf) is a measure of parallel simulation performance, which reveals how much faster the simulation is executed in parallel versus the sequential one [43]. Equation (3.7) describes how to calculate it. For instance, if the simulation execution time in parallel is 3 s and in the sequential one 30 s, the speed-up factor is 10.

$$suf = \frac{sst}{pst} \tag{3.7}$$

The efficiency (ef) describes where the improvements would be useful [2090]. Equation (3.8) describes the efficiency as a function of the number of processing threads (p). It also represents

the relationship between the minimum theoretical execution time for a parallel implementation (sst/p) and the measured processing time for the parallel run $pst(p)$.

$$ef(p) = \frac{sst/p}{pst(p)} \tag{3.8}$$

Chapter 4

Masivo public transport routes simulation

In this chapter, we describe the components and the operational description of the developed public transport routes simulation called Masivo. Masivo is a public transport simulation software built in this research project to evaluate the new parallel simulation model proposed. This software is divided into three main components, as described in Figure 4.1. First, we have the Parameters Loading Module (PLM), which is a Python sequential module tat loads 2 CSV files with the information related to the OD matrix, stops, and routes information. Then, we have the Parallel Simulation Core (PSC), which runs in OpenCL, the parallel public transport route simulation model, by running each stop's operation in an independent work-item. Finally, we have the Results Statistics Module (RSM), which is a Python module that extracts the statistical information related to several passengers server, commute times, and simulation performance. The following subsections describe in deep these three components.

The full Masivo source code is available in the following public repository, including installation instructions: `https://github.com/jpruiz84/masivo`

To cover the concurrency execution of the PSC, first, we start briefing the OpenCL architecture, including the platform model, execution model, memory model, and programming model. Then, we describe the Masivo three main components, which are PLM, PSC, and RSM.

4.1 OpenCL architecture

In this section, we present an overview of the OpenCL architecture used to run the proposed simulation model. OpenCL (Open Computing Language) is an open royalty-free standard a for general-purpose parallel programming across heterogeneous platforms consisting of central processing units (CPUs), graphics processing units (GPUs), field-programmable gate arrays (FPGAs), and other processors, giving software developers portable and efficient access to the power of these heterogeneous processing platforms [2091]. OpenCL consists of 4 hierarchy models (platform model, execution model, memory model, and programming model) described bellow.

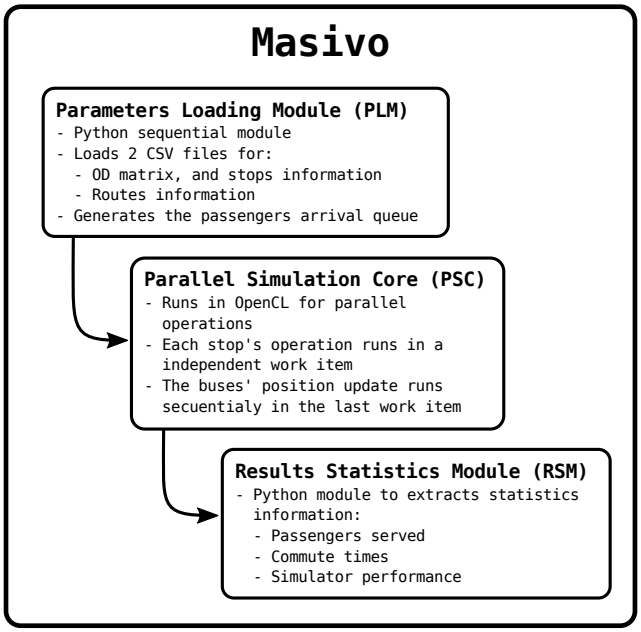


Figure 4.1: Masivo three main components

4.1.1 Platform model

The platform model consists of a host connected to one or more OpenCL devices. Indeed, an OpenCL device is divided into one or more Compute Units (CUs) that are divided into the processing elements (PEs), as described in Figure 4.2. An OpenCL application runs in the host. The OpenCL application submits commands from the host to execute computations on the PE within a device. The PE within a compute unit executes a single stream of instructions as a Single Instruction Multiple Data (SIMD), where a programming model in a kernel is executed concurrently on multiple processing elements, each with its data and a shared program counter. All processing elements execute a strictly identical set of instructions [2091].

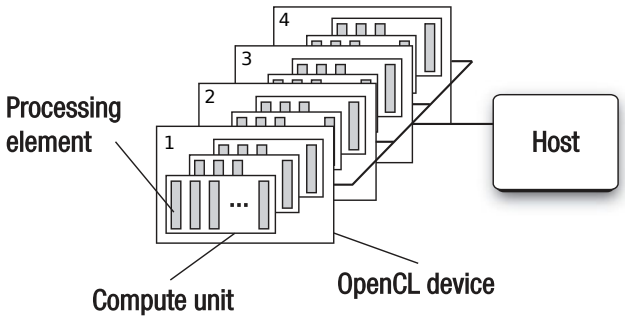


Figure 4.2: The OpenCL platform model with one host and four OpenCL devices. [2092]

4.1.2 Execution model

OpenCL execution program occurs in two parts: kernels that execute on the OpenCL devices and host program that executes on the host. The host program defines the context for the kernels and manages their execution. For OpenCL, the execution model is based on the parallel execution of the kernel over a 1D, 2D, or 3D grid, or NDRange ("N-Dimensional Range"). An instance of the kernel is executed for each point in this index space. This kernel instance is called a work-item and is identified by its point in the index space, which provides a global ID for the work-item. Each work-item executes the same code, but the specific execution pathway through the code and the data operated upon can vary per work-item [2091].

Work-items are organized into work-groups and identified within the work-group with a local ID. Work-groups are identified with a unique work-group ID. The work-items inside a work-group execute concurrently on the processing elements of a single compute unit. Figure 4.3 shows a simple example of work-items and work-groups organization. In this example, we have one dimension, 26 work-items divided into two work-groups. The work-items have a unique global ID that is independent of the work-group, for instance, the orange work-item with the data 2 in the example, has a global ID equal to 21. Also, each work-item has a local id that identifies it in the work-group, here the orange work-item has a local id equal to 8 inside the work-group with group id equal to 1.

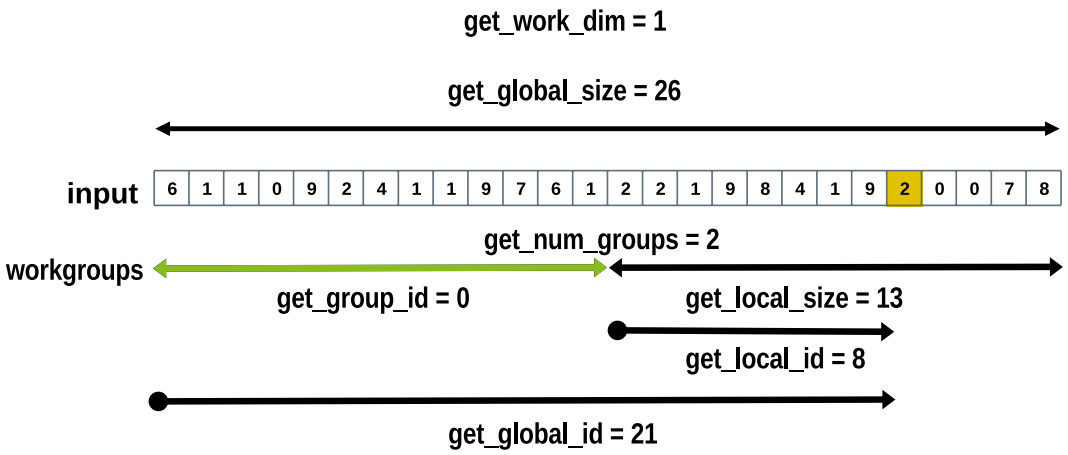


Figure 4.3: Execution model example with 2 works-groups, and 26 tatoal work items. [2093]

4.1.3 Memory model

The OpenCL memory model defines five distinct memory regions [2092]:

- **Host memory:** This memory region is visible only to the host. As with most details concerning the host, OpenCL defines only how the host memory interacts with OpenCL objects and constructs.
- **Global memory:** This memory region permits read/write access to all work-items in all work-groups. Work-items can read from or write to any element of a memory object in global memory. Reads and writes to global memory may be cached depending on the capabilities of the device.

- **Constant memory:** This memory region of global memory remains constant during the execution of a kernel. The host allocates and initializes memory objects placed into constant memory. Work-items have read-only access to these objects.

- **Local memory:** This memory region is local to a work-group. This memory region can be used to allocate variables that are shared by all work-items in that work-group. It may be implemented as dedicated regions of memory on the OpenCL device. Alternatively, the local memory region may be mapped onto sections of the global memory.

- **Private memory:** This region of memory is private to a work-item. Variables defined in one work-item private memory are not visible to other work-items.

The work-items run on the PEs and have their private memory. A work-group runs on a compute unit and shares a local memory region with the work-items in the group. To copy data explicitly, the host enqueues commands to transfer data between the memory object and the host memory.

4.1.4 Programming models

The programming model describes how we map parallel algorithms onto OpenCL. For this, OpenCL defines two different programming models: task parallelism and data parallelism. Also, a hybrid model of these two is supported.

- **Data parallel programing model:** It is defined as a sequence of instructions applied to multiple elements of a memory object. Here, there is a one-to-one mapping between the work-item and the element in a memory object over which a kernel can be executed in parallel. This is designed to be the OpenCL primary target.

- **Task parallel programing model:** In this mode, the problem is decomposed into sub-problems that run well on available compute resources.

4.2 Parameters Loading Module (PLM)

The Parameters Loading Modules (PLM) is a Python module that executes sequential operations to load and prepare the passenger arrival queue for the PSC. The PLM opens two CSV files, one with the information needed for the stop operations and others with the information needed for the bus operations, as described in Figure 4.4. The content of the two input files is described below.

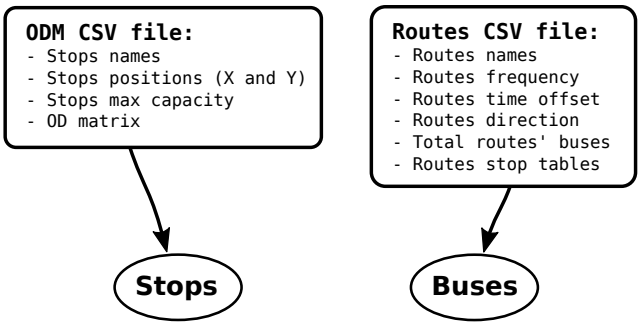


Figure 4.4: Masivo input parameters.

4.2.1 ODM CSV file

The ODM (OD Matrix) CSV file contains the information related to the operation of the stops. This information includes the names of the stops, stops' position (X and Y), stops' max capacity, and the OD matrix. Table 4.1 shows an example of an ODM file for a three stop system. The first column (stop_number) has the following list of numbers starting at zero to identify each stop. The second column (stop_name) presents a text string with the stop name due in real transport systems. Here, a name, instead of a number, is used to identify a stop or station. Then, the third and fourth columns indicate the X and Y position in meters. The fifth column shows the maximum passenger capacity at each stop. Finally, the last three columns indicate the OD matrix, where the first row of these columns represents the names of the destination stops.

Table 4.1: Origin-Destination Matrix (ODM) CSV example file with 3 stops' information.

Stop_Number	**Stop_Name**	**x_Pos**	**y_Pos**	**Max_Capacity**	**Stop_00**	**Stop_01**	**Stop_02**
0	Stop_00	400	1000	200	0	10	20
1	Stop_01	800	1000	200	10	0	10
2	Stop_02	1200	1000	200	20	10	0

4.2.2 Routes CSV file

The routes' CSV file contains the information related to the route's operation. This information includes the routes' set, names, routes' frequencies, routes' time offset, routes' direction, routes' notes, and stops' table. Table 4.2 shows an example of a routes' file with four routes' information. The first column (number) has the following list of numbers starting at zero to identify each route. The second column (name) presents the text string with the route name, as in a real transport system, names composed of letters and numbers are used to identify a route. The third column (freq.) indicates the route frequency in seconds, which represents how often a bus is dispatched for each route. The fourth column (offset) represents the route time offset in seconds, and it is the time when the first bus of each route is sent. The fifth column (buses) indicates the maximum number of buses available for each route. The sixth column (dir.) indicates the direction of this route, where W-E is west to east and E-W is east to west. The seventh column (notes) is used only for information proposes (not used by the PSC) and indicates, in this case, the type of route. Finally, the eighth column (stops_table) contains the stops' table, which indicates the stop stations where the bus has to stop to pick up or alight passengers.

Table 4.2: Routes CSV example file with 4 routes' information. Freq., frequency; Dir., direction.

Number	Name	Freq.	Offset	Buses	Dir.	Notes	Stops_Table
0	Route_00	300	100	50	W-E	all stops	Stop_00, Stop_01, Stop_02
1	Route_01	300	100	50	E-W	all stops	Stop_02, Stop_01, Stop_00
2	Route_02	900	100	50	W-E	express	Stop_00, Stop_02
3	Route_03	900	100	50	E-W	express	Stop_02, Stop_00

4.2.3 Passenger arrival queue generation

After loading the ODM and routes' CSV files, the PLM generates the passenger arrival queue (paq) for each stop from the OD matrix defined as D. The paq_i is an array that contains the passengers that will arrive at the stop during the simulation. The passengers are sorted by the arrival time, starting with the first passenger that arrives at the stop. Algorithm 2 describes the full process to generate the paq. First, in Line 2, we define the PASS_TOTAL_ARRIVAL_TIME as 3600 s. This means that the passengers will arrive at the stops from time 0 to 3600 s during the simulation. Then, in Line 3, we declare a for loop that will run in each of the stops i and then will run the rows of the OD matrix D. The passengers' queues are statics list, with a fixed size of STOP_MAX_PASS (by default, 10,000). Then, we initialize these lists, with a status value in each field that indicates the end of the list ($PASS\_STATUS\_END\_LIST$) and an $arrival\_time$ that is an unsigned short (UINT16) variable to the maximum possible value. This initialization is done by the operation performed in the loop from Lines 4 to 8.

Algorithm 2 Passenger arrival queue generation algorithm.

```
1:  procedure GENERATEPAQ
2:      PASS_TOTAL_ARRIVAL_TIME ← 3600;
3:      for i ← 0 to total_stops do
4:          for j = 0 to STOP_MAX_PASS do
5:              pwq_i[j].status = PASS_STATUS_END_LIST;
6:              paq_i[j].status = PASS_STATUS_END_LIST;
7:              paq_i[j].arrival_time = UINT16_MAX;
8:          end for
9:
10:         for j = 0 to total_stops do
11:             for k = 0 to D_[i,j] do
12:                 paq_i[j].orig_stop = i;
13:                 paq_i[j].dest_stop = j;
14:                 paq_i[j].arrival_time = PASS_TOTAL_ARRIVAL_TIME × k/D_[i,j];
15:             end for
16:         end for
17:         Sort paq_i by arrival_time;
18:     end for
19: end procedure
```

Later, in Line 10, we define a for loop to cover all destination stops. This will run the columns

of the OD matrix D. In Line 11, we set another for loop that will run for each passenger that will travel from stop index i to stop index j. In Lines 12 to 14, we set the passenger's origin stop $paq_i[j].orig\_stop$, the destination stop $paq_i[j].dest\_stop$, and the arrival time $paq_i[j].arrival\_time$. Finally, after the full list of passengers is generated for the stop i, we sort the passengers of paq_i by the arrival time. With this, the PSC can process paq efficiently, as we will discuss later.

The passengers arrival time has been distributed uniformly from the time 0s to the PASS_TOTAL_ARRIVAL_TIME. In this way, we will have the same flux of passengers to the stop during the arrival time. Also, if we want to modify the passenger arrival time distribution, we can modify the line 14 setting a arrival time that fix to predefined distribution, such as a distribution that simulate a crowd of passengers arriving to the stops during 15 minutes.

4.3 Parallel Simulation Core (PSC)

The Parallel Simulation Core (PSC) runs in an OpenCL kernel the passenger operations and the buses' position update. The simulation tick is 1 s (this means that all simulation components are updated every 1 s). Each passenger has a data structure that contains the data needed for his operations. Figure 4.5 shows the passengers' operations and the passengers data information. Each passenger has an ID that identifies him/her in the system; furthermore, the origin and destination stop numbers that indicate at which stop the passenger has arrived and at which stop he/she will alight. The arrival time is the time in the simulation that indicates when the passenger has arrived, and the alight time indicates when the passenger has alighted. The status points out the actual status of the passenger inside the simulation (to arrive, arrived, on the bus, alighted, or empty). The empty status means that this space is free for another passenger, such as a seat on the bus. This passenger structure uses 13 bytes of data per passenger.

The stops are defined in the simulator by an array of structures. As described in Figure 4.5, each element inside the stops' array has a stop number. Furthermore, they include the stop position in the map, total passengers, the last empty index, which indicates which was the last space empty in the waiting queue, and the passengers' queues. Second, we include the arrival queue for passengers that will arrive at the stop. Third is the waiting queue for passengers that have arrived at the stop and are waiting for the bus. Finally, there is the alight queue for passengers that have finished the trip and have alighted at the stop. Each stop structure uses 130 KB of data.

Next, we have an array of structures that describes the buses in the simulator. As shown in Figure 4.5, each element inside the buses' array has a bus number. Besides, we include the current stop index, which indicates at which stop the bus is, and the last stop index, which indicates which was the last stop where the bus stopped. Similarly, we incorporate here the stops' arrays that have the stops' index where the bus will stop to pick up or alight passengers. Finally, we include the total number of passengers on the bus and the passengers' array that has the data of the passengers that are on the bus.

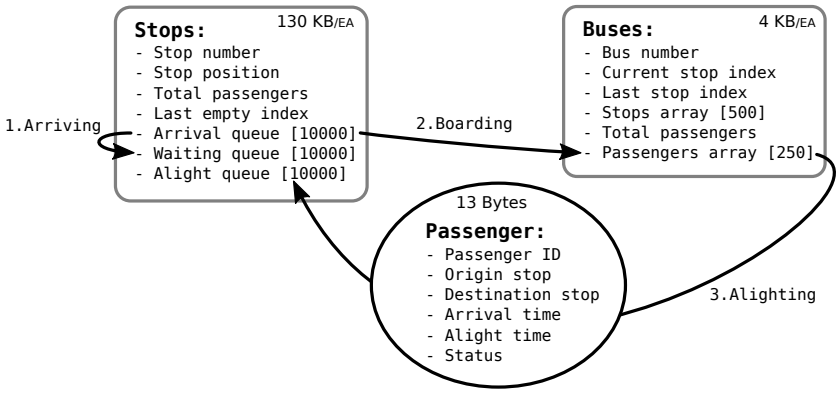


Figure 4.5: Masivo simulation passenger operations.

Moreover, in Figure 4.5, we see the three passengers' operations (1, arriving; 2, boarding; 3, alighting). During the arriving, the passenger passes from the arrival queue to the waiting queue at the origin stop. During the boarding, the passenger moves from the origin stop waiting queue to the bus passenger array. Finally, during the alighting, the passengers move to form the bus's passenger array to the alight queue at the destination stop. These passengers' move operations are optimized to run efficiently in OpenCL and are described in the following subsections.

4.3.1 Passenger arriving

In the passenger arriving operation, the passengers arrive at the stop at the arrival time. Algorithm 3 describes this process. First, we have an infinite while loop that breaks when there are no more passengers that will arrive at the stop in the given simulated time. In Line 2, we check if the total number of passengers remaining in paq is zero. If yes, we break the while loop. In Line 6, we extract the working index (w_index) of the passengers' arrival queue (paq) in w. This working index represents the last passenger's index that has been removed from paq. Then, in Line 9, if the arrival time of a passenger that we are processing $paq.p[w].arrival_time$ is greater than the actual simulation time, we do not process this passenger yet. Hence, we break the while loop. Due to the passengers in paq being sorted by $arrival_time$, we do not need to process the next passengers, because we already know that $arrival_time$ will be greater than sim_time.

Algorithm 3 Passengers' arriving operation at stop n, where passenger arrival queue *paq* and passenger waiting queue *pwq* are specific for stop n.

```
1:  while TRUE do
2:      if paq.p[l].total = 0 then
3:          break;
4:      end if
5:
6:      w ← paq.w_index;
7:      if paq.p[w].arrival_time > sim_time then
8:          break;
9:      end if
10:
11:     l ← pwq.last_empty;
12:     pwq.p[l] ← paq.p[w];
13:     pwq.p[l].status ← ARRIVED;
14:     pwq.last_empty ← pwq.last_empty + 1;
15:     pwq.last_total ← pwq.total + 1;
16:
17:     paq.p[l].status ← PASS_STATUS_EMPTY;
18:     paq.p[l].w_index ← paq.p[l].w_index + 1;
19:     paq.p[l].total ← paq.p[l].total − 1;
20:
21: end while
```

Thus, we move the passenger from the passenger arrival queue (*paq*) to the passenger waiting queue (*pwq*) only if the conditions of Lines 2 and 7 are not fulfilled. If we have a valid passenger with $arrival_time$ equal to or less than the simulation time, we move it. For this, in Line 11, we extract the *pwq* last empty index, which indicates the index of the last empty space in *pwq*. Then, we assign the actual processing passenger in the arrival queue $paq.p[w]$ to the last empty space in the waiting queue $pwq.p[l]$. Latter, in Lines 13–15, we update the passenger status, and we increment the last empty index and the total counter for *pwq*. In Lines 17–19, we update the *paq* passenger's status to PASS_STATUS_EMPTY, we update the w_index of *paq*, to process the next passenger in the next iteration, and we decrement the total counter of passengers in *paq*

4.3.2 Passenger boarding

The passenger boarding operations run concurrently at each stop. Algorithm 4 describes the boarding operations for the stop n. For this, in Line 1, we start with a main for loop, then run for all the buses. Then, in Line 2, we have an if that only lets us process the bus passenger array (*bpa*) that is at the current stop. In Line 3, if the total number passengers in the waiting queue is zero (*pwq.total*), we brake, and we do not process more buses, because we do not have passengers at this stop waiting for boarding. In Line 6, we check if the total number of passengers of bus $bpa[j]$ has reached the maximum BUS_MAX_PASS (the bus is full). If yes, we continue to process the next bus.

At this point, in Line 9, we know that passengers are waiting at the stop, and the bus is not

full. Therefore, we check for each passenger at the stop to check which of them needs to board the actual bus. For this, in Line 9, we set a temporal variable *last_empty_seat_in_bus* to zero. This variable indicates which is the last seat on the bus that is empty. In this way, if there is more than one passenger in the stop to board the bus, we will not start from the beginning of the seats to check which is empty for each passenger.

To check if a passenger is at the stop, in Line 10, we have a for loop, then it runs over passenger waiting queue until STOP_MAX_PASS, that is the last position of the queue (in this case, 10,000). The queue is a static list with a size of 10,000. We know that there will be no more than 10,000 passengers in this queue; the total number of passengers in this queue is always less than this size. To know if we have passed the last passenger that has arrived in the queue, we check that the passenger's status is PASS_STATUS_END_LIST. If yes, we break, and we finish checking for passengers to board at this stop. In Line 15, we check if the status of the passenger ($pwq[k]$) is PASS_STATUS_ARRIVED, which indicates that the passenger has arrived at the stop and is waiting for the bus. Then, in Line 16, we check if the destination stop of this passenger is in the stops' table of the bus that we are processing. If yes, in Line 17, we have a for loop that checks the next empty seat on the bus, with the if condition in Line 18. If the position is empty on the bus, we move the passenger from the waiting list to the bus empty seat in Line 19. In Lines 20 and 21, we update the passenger's status to PASS_STATUS_IN_BUS, and we increment the total number of passengers on the bus. In Lines 22 to 23, we update the status of the empty space in the *pwq*, and we decrement the total number of passengers at the stop. Finally, in Line 24, we update the temporal variable *last_empty_seat_in_bus* to l, so that when we process the next passenger at this stop in this simulation time iteration, we do not start from the beginning of the bus seats, which we already know are not empty.

Algorithm 4 Passengers' boarding operation at stop n, where *pwq* is the passenger waiting queue specific for the stop n.

```
1: for j ← 0 to total_buses do
2:     if stop_num = bpa[j].curr_stop then
3:         if pwq.total = 0 then
4:             break;
5:         end if
6:         if bpa[j].total ≥ BUS_MAX_PASS then
7:             continue;
8:         end if
9:         last_empty_seat_in_bus ← 0;
10:        for k ← 0 to STOP_MAX_PASS do
11:            if pwq[k].status = PASS_STATUS_END_LIST then
12:                break;
13:            end if
14:
15:            if pwq[k].status = PASS_STATUS_ARRIVED then
16:                if pwq[k].dest_stop in bpa[j].stops_table then
17:                    for l ← last_empty_seat_in_bus to BUS_MAX_PASS do
18:                        if bpa[j].bpl[l].status = PASS_STATUS_EMPTY then
19:                            bpa[j].bpl[l] ← pwq[k]
20:                            bpa[j].bpl[l].status ← PASS_STATUS_IN_BUS
21:                            bpa[j].total ← bpa[j].total + 1
22:                            pwq[k].status ← PASS_STATUS_EMPTY
23:                            pwq.total ← pwq.total − 1
24:                            last_empty_seat_in_bus ← l
25:                            break;
26:                        end if
27:                    end for
28:                end if
29:            end if
30:
31:        end for
32:    end if
33: end for
```

4.3.3 Passenger alighting

The passenger alighting operations also run concurrently at each stop. Algorithm 5 describes the boarding operations for the stop n. For this, in Line 1, we start with a main for loop that runs for all the buses. Then, in Line 2, we have an if that only lets us process the bus passenger array (*bpa*) that is in the current stop. In Line 3, we have an if that only lets us process buses that have more than zero passengers. In this way, at this point, we know that the bus is at the stop, and we have at least one passenger there. Then, in Line 5, we have another for loop that

runs for all the bus's seats. Later, the if condition in Line 6 checks if there is a passenger in the actual processing seat. Next, the if condition in Line 7 check if the passenger's destination stop is the same as the actual stop. If yes, we know that the passenger must alight from the bus.

Algorithm 5 Passenger alighting operation at stop n, where passenger waiting queue pwq and passenger alight queue plq are specific for stop n.

```
1:  for j ← 0 to total_buses do
2:      if stop_num = bpa[j].curr_stop then
3:          if bpa[j].total > 0 then
4:
5:              for k ← 0 to BUS_MAX_PASS do
6:                  if bpa[j].bpl[k].status = PASS_STATUS_IN_BUS then
7:                      if bpa[j].bpl[k].dest_stop = pwq.stop_num then
8:                          l ← plq.total;
9:                          plq[l] ← bpa[j].bpl[k];
10:                         plq[l].status ← PASS_STATUS_ALIGHTED;
11:                         plq[l].alight_time ← sim_time;
12:                         plq.total ← plq.total + 1;
13:
14:                         bpa[j].bpl[k].status ← PASS_STATUS_EMPTY;
15:                         bpa[j].total ← bpa[j].total − 1;
16:                     end if
17:                 end if
18:             end for
19:
20:         end if
21:     end if
22: end for
```

To alight the passenger from the bus to the stop, first in Line 8, we get the last empty index of the passenger alight queue (plq) for the temporal variable l. Next, in Line 9, we move the passenger from the bus $bpa[j].bpl[k]$ to the alighting stop $pql[l]$. Later, in Lines 10 to 11, we update the passenger status to PASS_STATUS_ALIGHTED, we set the alight time, and we increment the total number of passengers in the alight queue. Finally, in Lines 14 and 15, we set the status of the empty seat on the bus to PASS_STATUS_EMPTY, and we decrement the passengers' total number for this bus.

4.3.4 Buses position update

The buses' position update runs sequentially per bus in an independent OpenCL work item. This position update consists of moving the bus across the stops and holding the bus at the stops inside the stop table for a fixed time in seconds. Algorithm 6 shows the operations for the bus position update. First, in Line 1, we have a for loop to run for all the buses. Then, in Line 2, we check if we have to start a new bus according to the route frequency and time offset. In Line 4, we check if the bus is already at a stop. If yes, we decrement $in\_the\_stop\_counter$, which

indicates how many seconds are remaining for the bus to be held at the stop. In Line 6, we check that *in_the_stop_counter* is zero. If yes, we set *in_the_stop* to FALSE, indicating that the bus has finished the holding time at the stop.

Algorithm 6 Bus update position operations.

```
1:  for i ← 0 to total_buses do
2:      check_if_start_the_bus(bus[i]);
3:
4:      if bus[i].in_the_stop = TRUE then
5:          bus[i].in_the_stop_counter ← bus[i].in_the_stop_counter − 1;
6:          if bus[i].in_the_stop_counter = 0 then
7:              bus[i].in_the_stop = FALSE;
8:          end if
9:      end if
10:
11:     if bus[i].in_the_stop = FALSE then
12:         bus[i].curr_pos ← bus[i].curr_pos + TRAVEL_SPEED;
13:     end if
14:
15:     if bus[i].curr_pos = next stop window then
16:         bus[i].curr_stop ← next_stop_i;
17:         bus[i].in_the_stop ← TRUE;
18:         bus[i].in_the_stop_counter ← BUS_STOPPING_TIME;
19:     end if
20: end for
```

Then, in Line 11, we check if the bus is not at the stop. If it is not held at the stop, we increment the current position (*curr_stop*) according to TRAVEL_SPEED. Finally, we check in Line 15 if the bus is in the stop window of the next stop. If yes, we update the *curr_stop* and *in_the_stop* variables accordingly; also, we set *in_the_stop_counter* to BUS_STOPPING_TIME, which by default is 20 s.

4.4 Results Statistics Module (RSM)

The Results Statistics Module (RSM) is a Python module that extracts the statics information results from the executed simulation. It extracts the number of passengers served, the passengers' commute time, and the simulation performance. Masivo saves this information in the result folder, including CSV files and statistics graphs.

4.4.1 Passengers served information

When the simulation is done, each of the stops has a passenger alight queue, which contains the full passenger structure information (passenger ID, origin and destination stops, arrival and alight time, and status), as described in Figure 4.5. Masivo saves this information and statics about this information in the following output files.

- **total_passengers_results.csv:** contains all the information (passenger ID, origin and destination stops, arrival and alight time, and status) of all passengers inside the simulation.
- **served_passengers_per_stop.csv:** describes per stop the total number of passengers waiting for a bus, the expected total input passengers, the total alight passengers, the total expected alight passengers, and the alighted passengers' percentage.
- **served_passengers_per_stop.eps:** graphs the total alighted passengers contrasted with the remaining passengers expected per stop.
- **commute_time_per_stop.eps:** graphs the average commute time of the alighted passengers per destination stop and per travel direction. This graph is useful to see how the commute time is affected at a specific destination stop depending on traffic congestion on the road.

4.4.2 Performance information

To know the simulation performance, Masivo saves useful simulation timings and host computer status information. These data are stored in the following files:

- **performance_timeline.csv:** contains the real-time simulation factor over time, with a sampling frequency of 100 s of the simulation. Furthermore, this file contains information related to CPU usage and CPU operation frequency over time.
- **performance_timeline.eps:** graphs the real-time factor over time, the real-time factor low-pass filtered signal, the CPU usage, and the CPU operation frequency.
- **simulation_brief.csv:** contains all simulation configured parameters, total simulation outputs, and total performance indicators. In particular, as inputs, this file contains the buses' average travel speed, bus max passengers, bus stopping time, end simulation time, ODM file, passenger total arrival time, routes' file, and stop to bus windows' distance. As outputs, we find here total alighted expected passengers, total alighted passengers, total alighted passenger percentage, total average commute time, total simulated buses, total simulated passengers, total routes, and total stops. Finally, for the total performance indicators, we include in this file the average CPU usage, average real-time factor, total simulation execution time, OpenCL device name and compute units used, and the limit of the max OpenCL compute units.

4.5 3D system visualization output

For validation purposes, a 3D system visualization output was integrated into Masivo. This visualization system is based on a Python 3D engine called Panda3D. When enabled, a separate thread runs the 3D visualization, with a running interval of 30 fps. In each frame update, the buses' position, buses' occupied seats, stops' alighted passengers, and stops' waiting passengers values are updated from the PSC. Figure 4.6 shows this 3D output interface. Here, the stops are represented with a blue container, which has a horizontal red bar that indicates the percentage of passengers in the waiting queue relative to the maximum stop passenger capacity. The vertical

purple cylinder represents the percentage of alighted passengers relative to the total expected alight passengers. The bus has a horizontal red bar, which represents the percentage of occupied seats relative to the maximum bus passenger capacity.

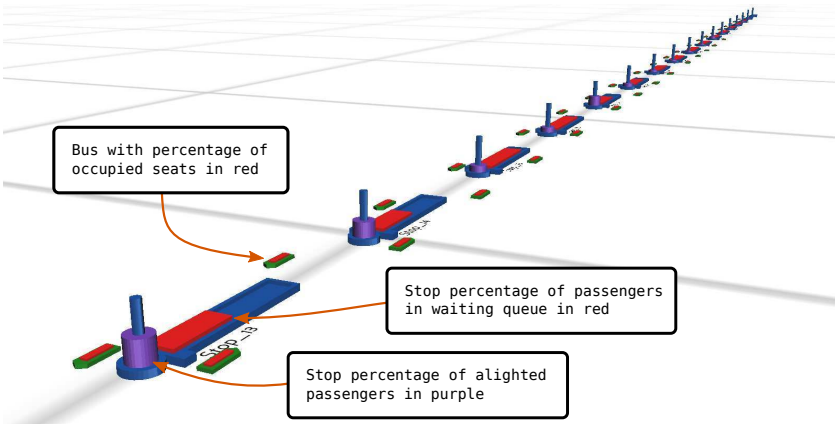


Figure 4.6: Masivo 3D game engine simulation output.

4.6 Validation simulator

A validation simulator was built only using Python (called here Pure Python) with dynamic arrays (to emulate passenger's queues). This Pure Python simulator helped to get results that ensured the correct operation of the routes inside an origin-destination demand and then compared these results with the parallel simulator. In this simulator, contrary to the Masivo PSC, the boarding and alighting operations were performed per bus that was held at a stop and not at the stop.

The correct behavior for this simulator was validated with the 3D system visualization output. For this, a three stop small public transport simulation system was simulated. The ODM matrix used here is described by Equation (4.1), totaling 80 passengers. The passengers arrived at the stops from Time 0 to 3600 s.

$$\text{ODM matrix} = \begin{bmatrix} 0 & 10 & 20 \\ 10 & 0 & 10 \\ 20 & 10 & 0 \end{bmatrix} \tag{4.1}$$

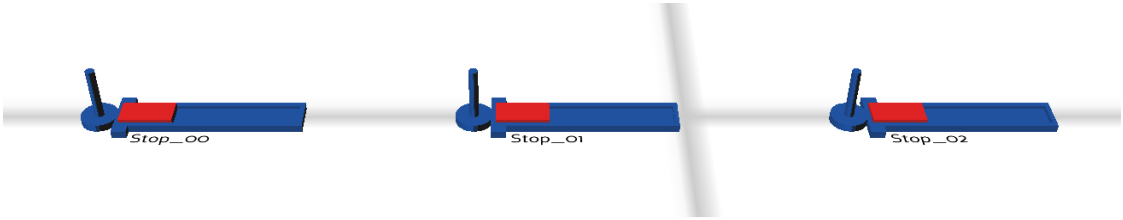
Two routes, with a 15 min frequency, were used for this system. The routes' files are described by Table 4.3.

Table 4.3: Routes used to validate a small 3 stop public transport system.

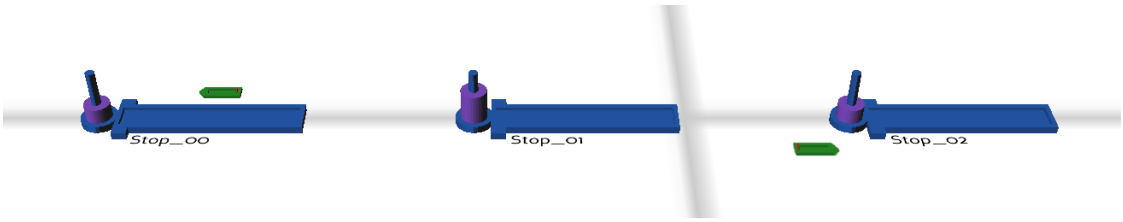
Number	Name	Freq.	Offset	Buses	Dir.	Notes	Stops_Table
0	Route_00	900	950	50	W-E	all stops	Stop_00, Stop_01, Stop_02
1	Route_01	900	950	50	E-W	all stops	Stop_02, Stop_01, Stop_00

Figure 4.7 shows the 3D visualization output for three different simulation times. Figure 4.7a shows the stops at the time 800 s of the simulation. Here, some passengers have arrived at the

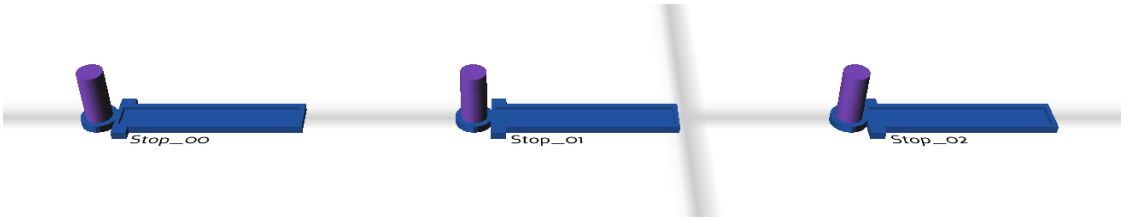
stops, but the buses have not departed yet. Figure 4.7a shows the simulation at the time of 1900 s. Here, some passengers have arrived at their destination stops. Furthermore, we see two buses moving passengers. Finally, Figure 4.7c shows the end of the simulation, where all passengers have arrived at their stops.



(a)



(b)



(c)

Figure 4.7: 3D visualization for a three stops small public transport system. (**a**) at 800 s simulation time (**b**) at 1900 s simulation time (**c**) at 7200 s end simulation time.

Furthermore, Figure 4.8 shows the total alighted and not alighted passengers at each stop. Here, we note that all passengers (80 of 80 expected) alighted at their destination stops.

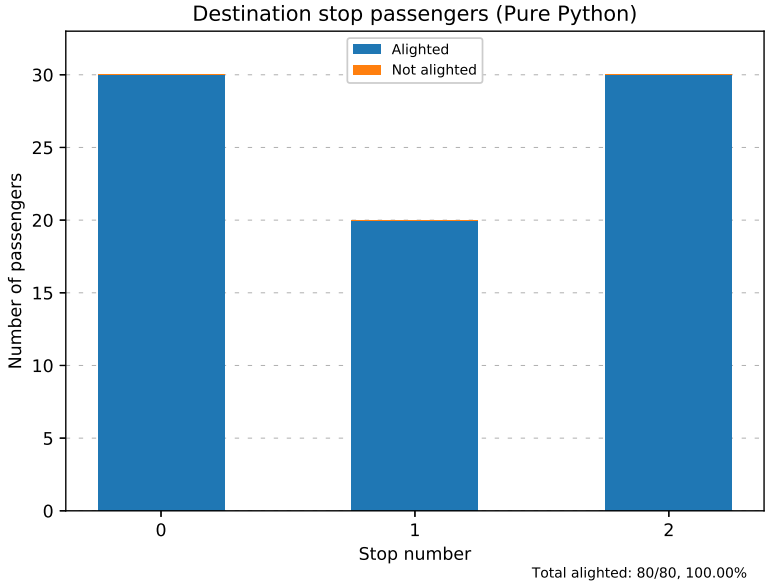


Figure 4.8: Alighted passengers results for a three stop validation system in Pure Python.

Finally, this validation simulation also calculated the average commute for the passengers per destination stop and travel direction, as shown in Figure 4.9. Here, we note that the commute time for corner stops (Stop_00 and Stop_02) was greater than the commute time of the center stop (Stop_01). This was because, for instance, Stop_02 received passengers from the closest stop Stop_00 and the furthest stop Stop_01. Meanwhile, Stop_01 received a passenger for the closer stops Stop_00 and Stop_02; hence, the passengers' average commute time was lower.

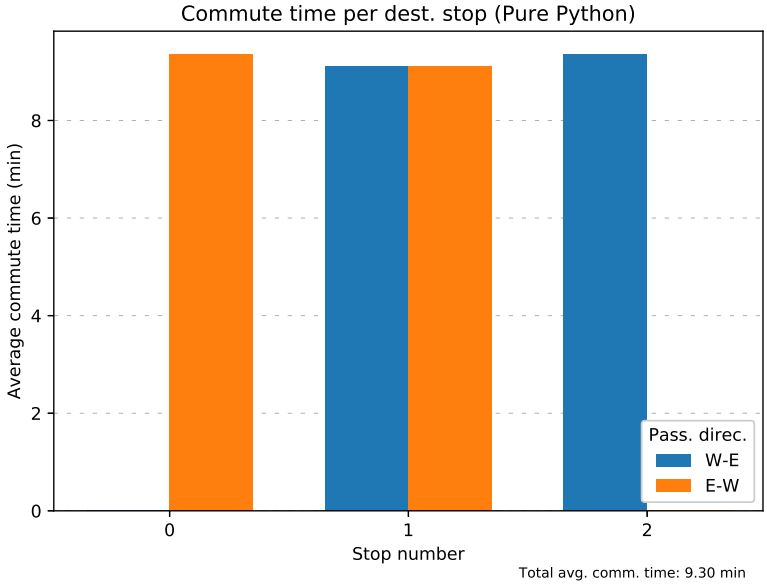


Figure 4.9: Commute time per stop for a three stop validation system in Pure Python. The abbreviation "dest. stop" refers to destination stop, "Pass. direc." refers to passenger direction, "W-E" refers to West to East direction, and 'E-W" refers to East to West direction.

Other validation scenarios output files are included in the Appendix B.

Chapter 5

Results

In this chapter, we discuss the simulation model results. First, we present the results for the validation process, where we compare the Masivo PSC outputs with the Pure Python validation simulator. Then, we show the performance results.

5.1 Validation results

For the validation of the Masivo PSC, four different scenarios were created. These scenarios, with the same conditions, were simulated in the Masivo PSC and the Pure Python validation simulator. Output simulation results related to alighted passengers per stop and the commute time were compared.

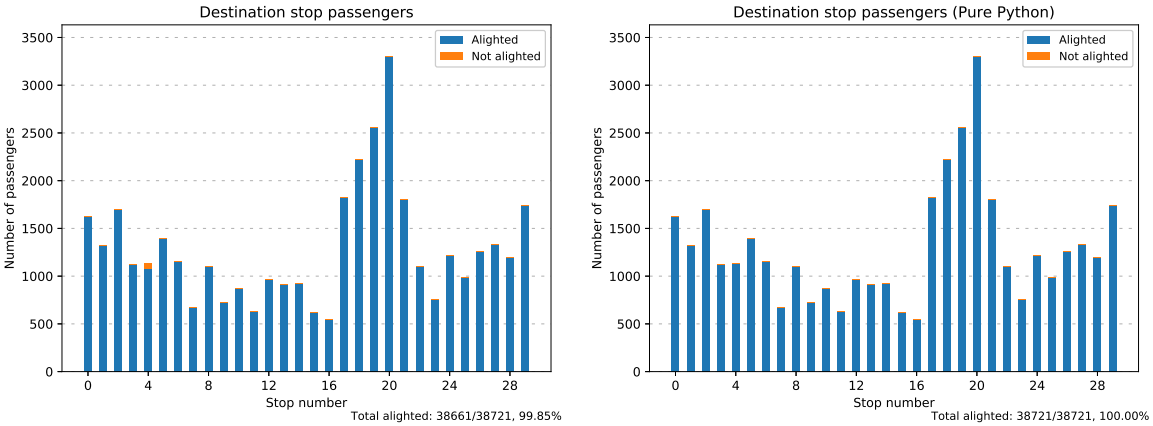
5.1.1 Scenario 1, 30 stops, 2 routes at 54 Km/h

The simulation conditions for Scenario 1 are summarized in Table 5.1. The two routes pick up and alight passengers from all stops, with a bus departing frequency of 1 min. The first route goes from west to east, and the second one goes from east to west. The separation of the stops is 400 m, totaling a line length of 12 km for the 300 stops. This scenario was based on a full line of a BRT, such as the NQS line in Transmilenio BRT from Bogotá, Colombia. The BRTs use buses with average speed of 54 km/h, each bus capacity is 250, the average stooping time is 20 seconds, and maximum 40,000 passengers per hour per direction [2094].

Table 5.1: Scenario 1 simulation conditions.

Condition	**Value**
Bus average transit speed (km/h)	54
Bus maximum passengers	250
Bus stopping time (s)	20
End simulation time (s)	7200
Passenger total arrival time (s)	3600
Total passengers	38,721
Total routes	2
Total stops	30

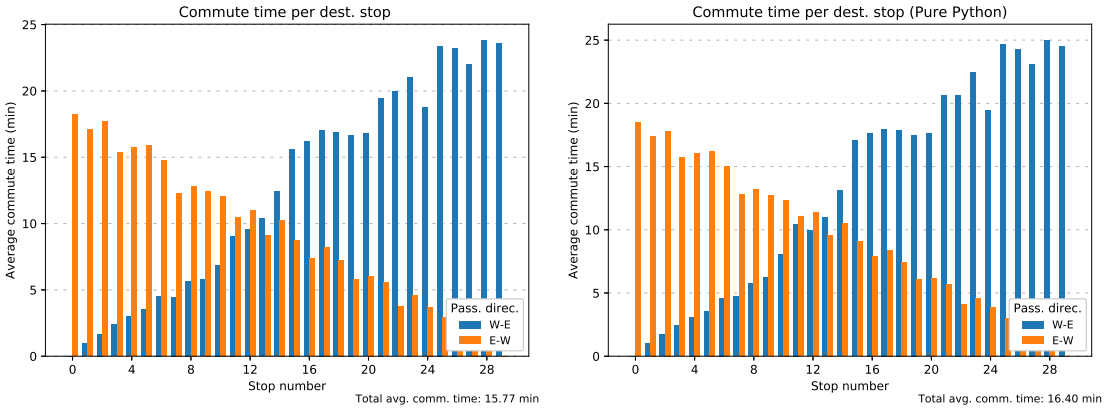
Figure 5.1 shows the alighted passenger numbers per stop and the total alighted passenger numbers and percentage. The percentage of alighted passengers for the Masivo PSC was 99.85% and 100.00% for the Pure Python validation simulator, giving an error of 0.15%.



(a) (b)

Figure 5.1: Alighted passengers per stop, 30 stops in Scenario 1. (**a**) Results from Masivo PSC. (**b**) Results from the Pure Python validation simulator.

Figure 5.2 shows the average passengers' commute time per destination and the total average commute time. Masivo PSC showed a total average commute time of 15.77 min. Meanwhile, the Pure Python validation simulator showed a total average commute time of 16.44 min, giving us an error of 0.52% relative to the total simulation time.



(a) (b)

Figure 5.2: Passengers' commute time per destination stop, 30 stops in Scenario 1. (**a**) Results from Masivo PSC. (**b**) Results from the Pure Python validation simulator. The abbreviation "dest. stop" refers to destination stop, "Pass. direc." refers to passenger direction, "W-E" refers to West to East direction, and 'E-W" refers to East to West direction.

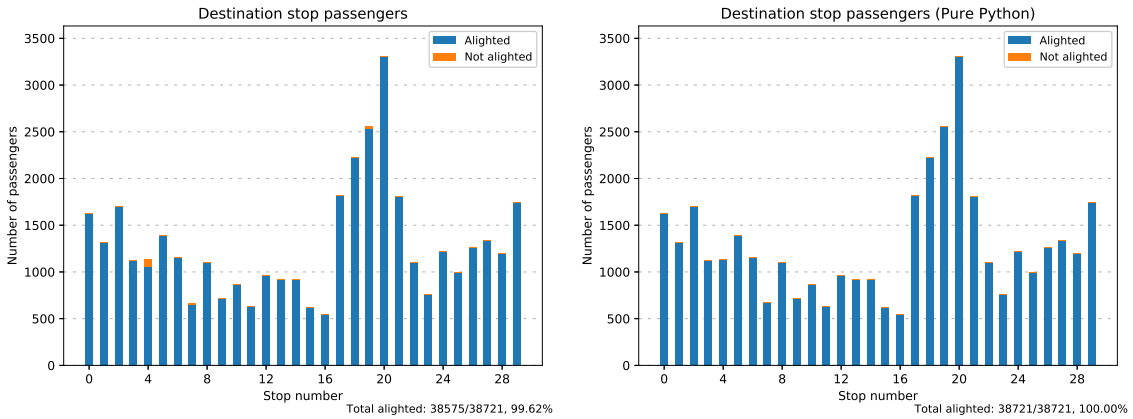
5.1.2 Scenario 2, 30 stops, 2 routes at 70 Km/h

The simulation conditions for Scenario 2 are summarized in Table 5.2, where the difference between this and Scenario 1 was the transit bus speed, increased from 54 km/h to 70 km/h. As the scenario 1, the scenario 2 was generated from the BRT one line system.

Table 5.2: Scenario 2 simulation conditions.

Condition	Value
Bus average transit speed (km/h)	70
Bus maximum passengers	250
Bus stopping time (s)	20
End simulation time (s)	7200
Passenger total arrival time (s)	3600
Total passengers	38,721
Total routes	2
Total stops	30

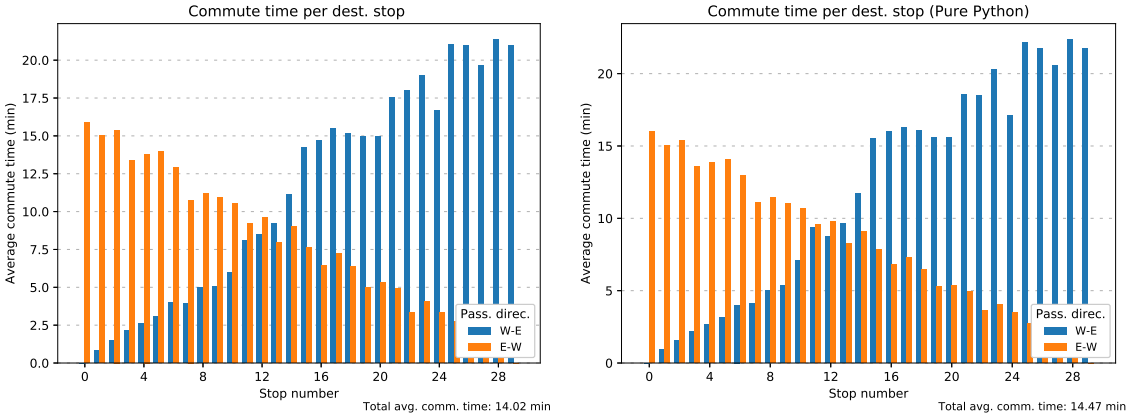
Figure 5.3 shows the alighted passenger numbers per stop and the total alighted passenger numbers and percentage. The percentage of alighted passengers for the Masivo PSC was 99.62% and 100.00% for the Pure Python validation simulator, giving an error of 0.38%.



(a) (b)

Figure 5.3: Alighted passengers per stop, 30 stops in Scenario 2. (**a**) Results from Masivo PSC. (**b**) Results from the Pure Python validation simulator.

Figure 5.4 shows the average passengers' commute time per destination and the total average commute time. Masivo PSC showed a total average commute time of 14.02 min. Meanwhile, the Pure Python validation simulator showed a total average commute time of 14.47 min, giving us an error of 0.37% relative to the total simulation time.



(a) (b)

Figure 5.4: Passengers' commute time per destination stop, 30 stops in Scenario 2. (**a**) Results from Masivo PSC. (**b**) Results from the Pure Python validation simulator. The abbreviation "dest. stop" refers to destination stop, "Pass. direc." refers to passenger direction, "W-E" refers to West to East direction, and 'E-W" refers to East to West direction.

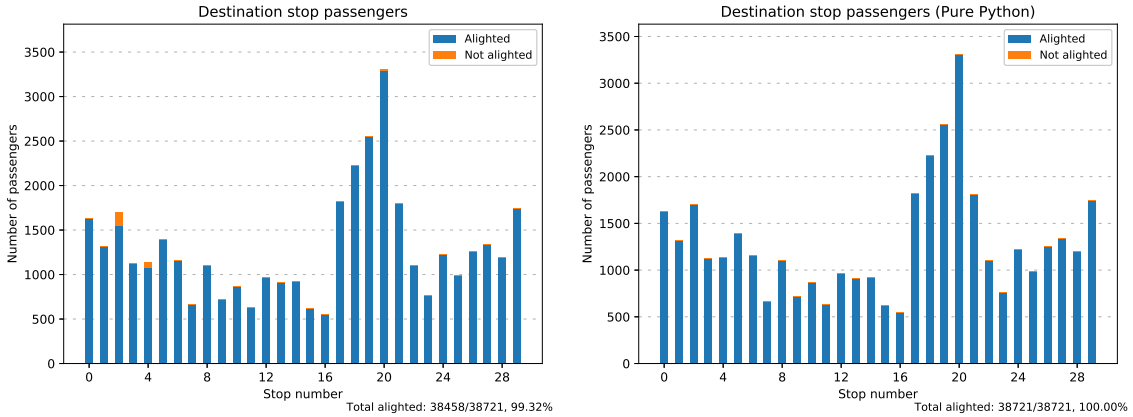
5.1.3 Scenario 3, 30 stops, 4 routes at 54 Km/h

The simulation conditions for Scenario 3 are summarized in Table 5.3, where the difference between this and Scenario 1 is the number of routes. As the scenario 1, the scenario 3 was generated also from the BRT one line system. Here, we have two new routes that do not stop at all stops. These new routes stop at the corners and in the downtown area where the demand is higher than the others. Both new routes have a frequency of 2 min. Precisely, Route 3 stops at Stop_00, Stop_01, Stop_02, Stop_03, Stop_18, Stop_19, Stop_20, Stop_21, and Stop_22. Meanwhile, Route 4 stops at Stop_29, Stop_28, Stop_27, Stop_26, Stop_22, Stop_21, Stop_20, Stop_19, Stop_18.

Table 5.3: Scenario 3 simulation conditions.

Condition	Value
Bus average transit speed (km/h)	54
Bus maximum passengers	250
Bus stopping time (s)	20
End simulation time (s)	7200
Passenger total arrival time (s)	3600
Total passengers	38,721
Total routes	4
Total stops	30

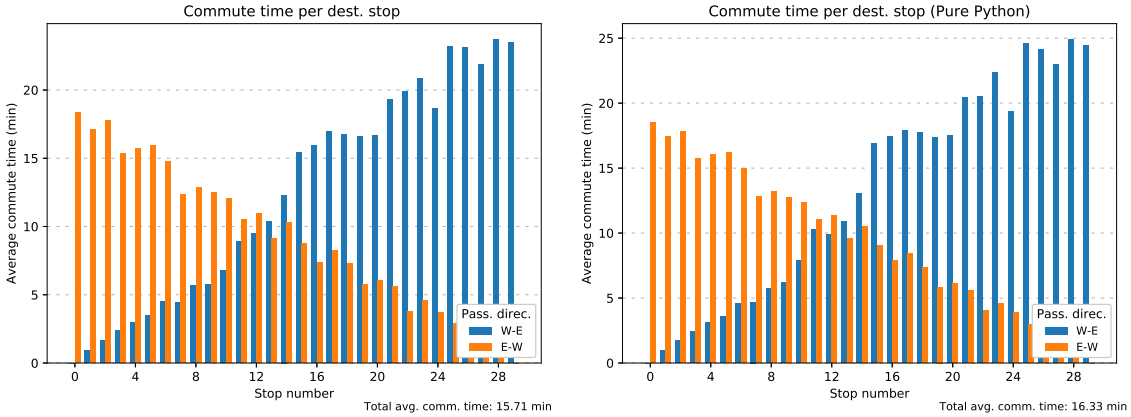
Figure 5.5 shows the alighted passenger numbers per stop and the total alighted passenger numbers and percentage. The percentage of alighted passengers for the Masivo PSC was 99.37% and 100.00% for the Pure Python validation simulator, giving an error of 0.63%.



(a) (b)

Figure 5.5: Alighted passengers per stop, 30 stops in Scenario 3. (**a**) Results from Masivo PSC. (**b**) Results from the Pure Python validation simulator.

Figure 5.6 shows the average passengers' commute time per destination and the total average commute time. Masivo PSC showed a total average commute time of 15.71 min. Meanwhile, the Pure Python validation simulator showed a total average commute time of 16.33 min, giving us an error of 0.52% relative to total simulation time.



(a) (b)

Figure 5.6: Passengers' commute time per destination stop, 30 stops in Scenario 3. (**a**) Results from Masivo PSC. (**b**) Results from the Pure Python validation simulator. The abbreviation "dest. stop" refers to destination stop, "Pass. direc." refers to passenger direction, "W-E" refers to West to East direction, and 'E-W" refers to East to West direction.

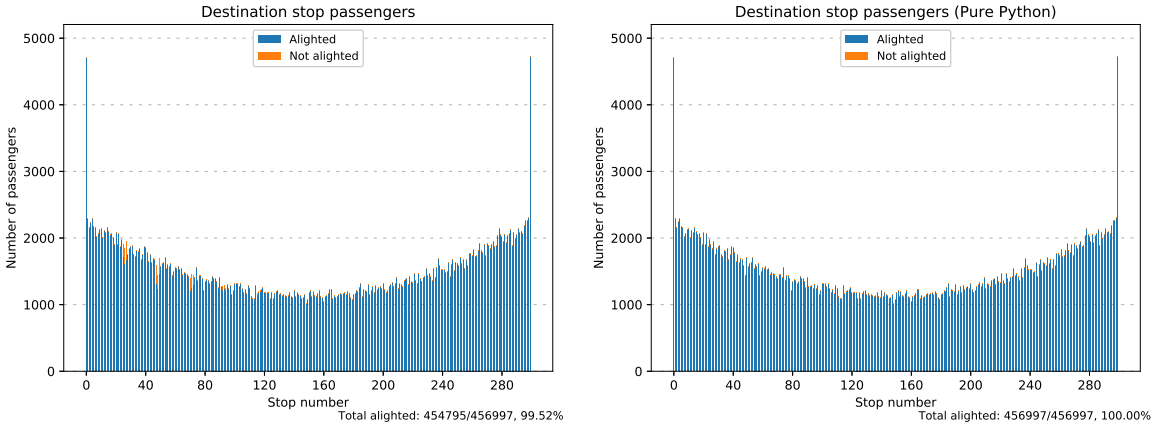
5.1.4 Scenario 4, 300 stops, 2 routes at 54 Km/h

The simulation conditions for Scenario 4 are summarized in Table 5.4. It consists of 300 stops, which have a constant distribution with more demand for longer distances plus a random number of passengers. Furthermore, corner stops have two times more demand than the others. The two routes pick up and alight passengers from all stops, with a bus departing frequency of 30 s. The first route goes from west to east, and the second one goes from east to west. The separation of the stops is 400 m, totaling a line length of 120 km for the 300 stops. Then, the end simulation time is 10 h, so that all passengers have enough time to finish traveling. This scenario was based on a worst case scenario from the limitation of the BRT (bus average speed of 54 km/h, each bus capacity is 250, the average stooping time is 20 seconds) and the size close to the world biggest metro system (London Underground 270 stops and 5 million daily passengers).

Figure 5.7 shows the alighted passenger numbers per stop and the total alighted passenger numbers and percentage. The percentage of alighted passengers for the Masivo PSC was 99.52% and 100.00% for the Pure Python validation simulator, giving an error of 0.48%.

Table 5.4: Scenario 1 simulation conditions.

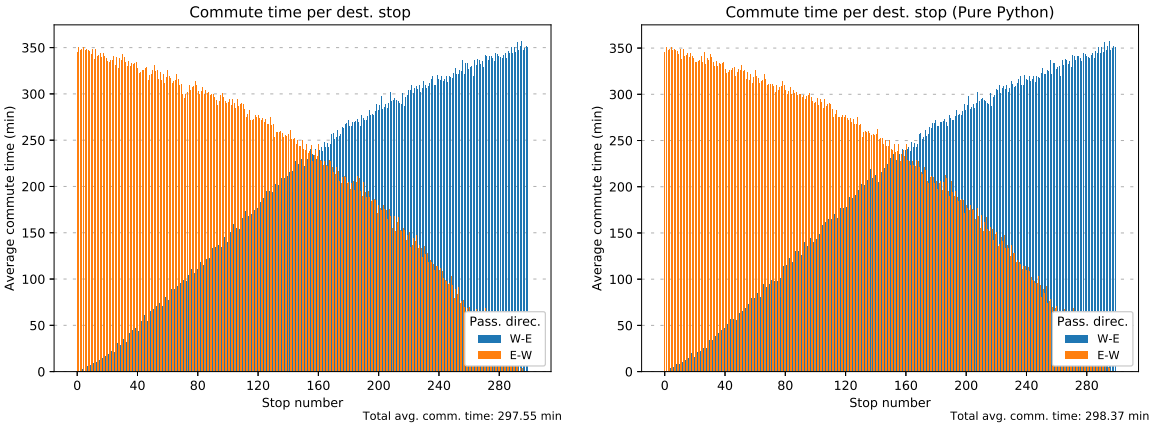
Condition	Value
Bus average transit speed (km/h)	54
Bus maximum passengers	250
Bus stopping time (s)	20
End simulation time (s)	36,000
Passenger total arrival time (s)	3600
Total passengers	456,997
Total routes	2
Total stops	300



(a) (b)

Figure 5.7: Alighted passengers per stop, 300 stops in Scenario 4. (**a**) Results from Masivo PSC. (**b**) Results from the Pure Python validation simulator.

Figure 5.8 shows the average passengers' commute time per destination and the total average commute time. Masivo PSC showed a total average commute time of 297.55 min. Meanwhile, the Pure Python validation simulator showed a total average commute time of 298.37 min, giving us an error of 0.13% relative to the total simulation time.



(a) (b)

Figure 5.8: Passengers' commute time per destination stop, 300 stops in Scenario 4. (**a**) Results from Masivo PSC. (**b**) Results from the Pure Python validation simulator.

5.2 Performance

The performance simulation execution was performed in a dedicated server rented from 1&1 IONOS (`https://www.ionos.com/servers/dedicated-servers`). The specification of the rented server is described in Table 5.5. Before each performance test, the Linux CPU scaling governors were set in performance mode, to enable the maximum operating frequency.

Table 5.5: IONOS dedicated server 4XL specifications.

Specification	**Value**
Type	Dedicated Server 4XL
CPU	Intel Xeon Gold 6210U
# of Cores	20
# of Threads	40
Processor Base Frequency	2.50 GHz
Max Turbo Frequency	3.90 GHz
Cache	27.5 MB
RAM	192 GB
HDD	2 × 4000 GB Hardware RAID 1
OS	Ubuntu 16.04

For the performance tests, the most complex simulation scenario (Scenario 4 previously tested) was used. This is a simulation scenario that has 300 stops and two routes. Table 5.6 describes the full list of conditions. It consists of 300 stops, which have a normal distribution with more demand for longer distances plus a random number of passengers. Furthermore, corner stops have two times more demand than the others. The two routes pick up and alight passengers from all stops, with a bus departing frequency of 30 s. The first route goes from west to east, and the second one goes from east to west. The separation of the stops is 400 m, totaling a line length of 120 km for the 300 stops. Then, the end simulation time is 10 h, so that all passengers have enough time to finish traveling.

Table 5.6: Simulation conditions for performance tests, Scenario 4.

Condition	**Value**
Bus average transit speed (km/h)	54
Bus maximum passengers	250
Bus stopping time (s)	20
End simulation time (s)	36,000
Passenger total arrival time (s)	3600
Total passengers	456,997
Total routes	2
Total buses	2400
Total stops	300

5.2.1 Pure Python validation simulator performance

The performance simulation of Scenario 4 was evaluated in the Pure Python validation simulator. Table 5.7 shows the performance output values. The total simulation execution time was near one hour (3303 s) for 10 h of simulation time. Then, the average real-time factor was 32.76 times faster than in real-time. Furthermore, we noted that due to this simulator being a sequential implementation, only one of the 40 processing threads was used, then only 2.19% of all the processing power was used.

Table 5.7: Pure Python simulator performance outputs for Scenario 4.

Performance Indicator	Value
Total simulation execution time (s)	3303.612
Average real-time factor	32.76
Average CPU usage (%)	2.19

Figure 5.9 shows the real-time factor (RTF) vs. the simulation time. Here, we note that the RTF starts at 780, and then, it has an exponential decline, getting values under 10 times. This decline is because the Pure Python simulator uses dynamic lists to handle passengers and buses. When the system starts, the number of passengers and buses is low. However, then, more passengers arrive at the stops, and more buses are dispatched. Hence, the systems have more elements to process, and the simulation speed decreases.

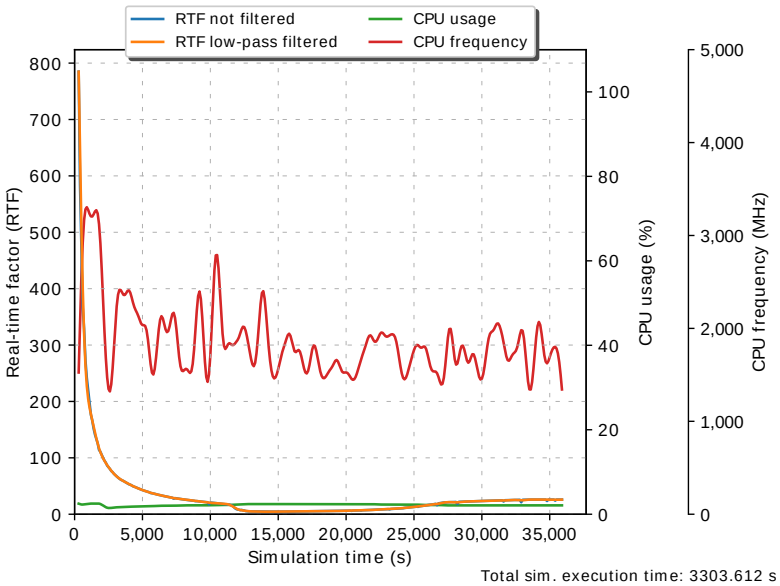


Figure 5.9: Real-time factor vs. simulation time for the Pure Python validation simulator with CPU usage percentage and CPU operation frequency.

Furthermore, in Figure 5.9, we see that the CPU usage was always near 2.5%, due to the fact that the sequential implementation will never use more than one processing thread. Finally,

the CPU frequency started at 3.2 GHz. However, because the CPU was not fully used, the OS decreased the CPU frequency during the simulation execution.

5.2.2 Masivo PSC performance

The Masivo Parallel Simulation Core (PSC) performance was also evaluated using Test Scenario 4. Table 5.8 shows the performance output values. The total simulation execution time was 11.822 s, 278 times faster than the Pure Python simulator. The average real-time factor was 3050 times faster than real-time, and the average CPU usage was 84.21%.

Table 5.8: Masivo PSC performance outputs for Scenario 4.

Performance Indicator	**Value**
Total simulation execution time (s)	11.882
Average real-time factor	3050.84
Average CPU usage (%)	84.21

Figure 5.9 shows the real-time factor vs. the simulation time. Here, we note that the RTF starts in 4300, and then, it has an exponential decline, stabilizing near 2500. This decline is because when the system starts, the number of passengers and buses is low, and the internal for loop that runs the statics list does not need to go to the end of the lists. Later in the simulation, more passengers arrive at the stops, and more buses are dispatched. Hence, the systems have more elements to process, and the simulation speed decreases. This decreasing is not as low as in the Pure Python simulator, due to the concurrent processing operations performed per stop. Finally, from the simulation time of 15,000, we see that the RTF is increasing due to the passengers arriving at the final destination, then there are fewer elements to process.

Figure 5.10 shows that the CPU usage is near 80%, due to all the cores being used most of the time. Finally, the CPU frequency started and sustained at 3.2 GHz, because the OS maintained this due to the high processing demand.

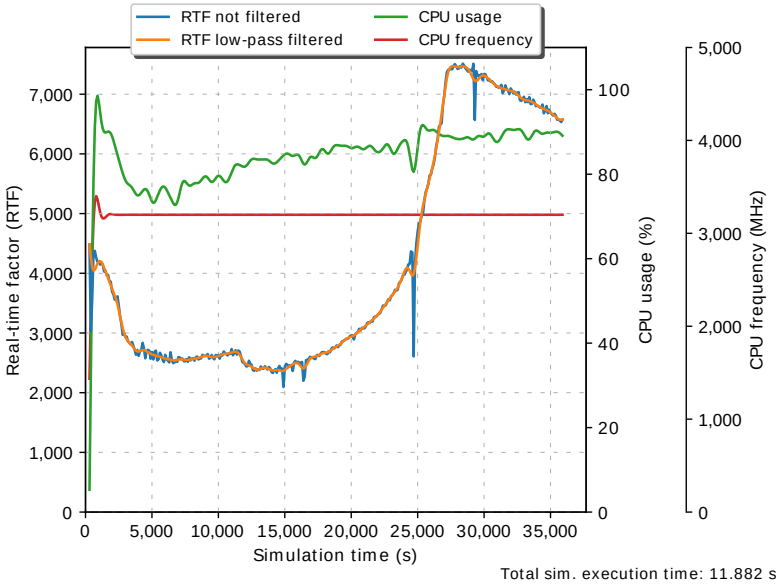


Figure 5.10: Real-time factor vs. simulation time for Masivo PSC with CPU usage percentage and CPU operation frequency.

As described in Section 3.4, the simulation performance indicators were extracted. Figure 5.11 shows these indicators for the simulation executed with the compute units limited from one to 40. These results helped us to identify the performance for the different numbers of processing units and the efficiency of the proposed model.

First, Figure 5.11a shows the simulation execution time vs. the compute units. We see here that the execution time required to run the 10 h simulation was reduced exponentially with more compute units. Nevertheless, we had a low limit, near 10 s, because there were operations in the model that were not parallelized, such as the position update of the buses. Second, Figure 5.11b shows the real-time factor, which also increased, with the number of cores reaching a final value near to 3000.

Next, Figure 5.11c has the same shape as the RTF, because it is a function also of the simulation execution time, but in this case, divided by the simulation execution time for one compute unit. We see here that the maximum speed up factor reached was 10.2 times faster than the sequential simulation. Finally, we have the efficiency in Figure 5.11d, which shows an efficiency of more than 50% for 10 or less compute units.

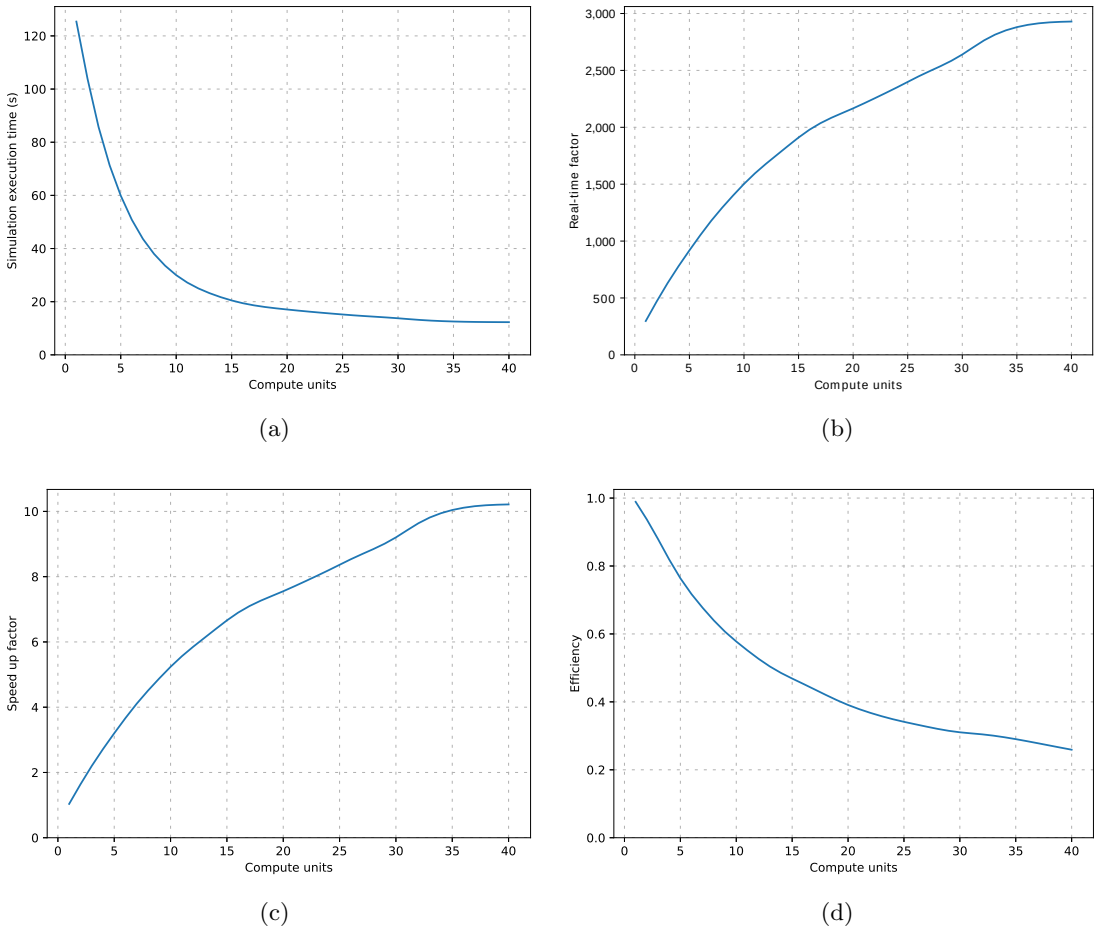


Figure 5.11: Simulation performance indicators vs. number of compute units. (**a**) Total parallel simulation execution time (pst). (**b**) Real-time factor (rtf). (**c**) Speed-up factor (suf). (**d**) Efficiency (ef).

In summary, Figure 5.12 shows the simulation execution time differences for the Masivo Pure Python validation simulator, and Masivo PSC limited to 1 compute unit and limited to 40 compute units running the simulation scenario 4. Here we noted that Masivo PSC with 1 compute unit runs more than 10 times faster than the Masivo Pure Python validation simulator. Also, we found that with 40 compute units, Masivo PSC runs 10 times faster than the simulation executed with 1 compute unit.

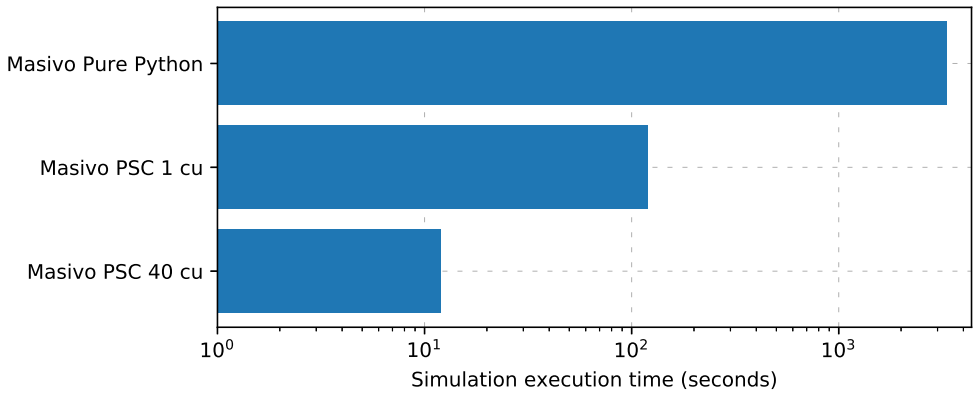


Figure 5.12: Simulation execution time comparative for the Masivo Pure Python validation simulator, Masivo PSC limited to 1 compute unit, and Masivo with 40 compute units.

Chapter 6

Conclusions and future work

A new simulation model for routes in public transport systems using parallel computing in IoT environments, called Masivo PSC, is presented. Masivo PSC works with a predefined public transport system conditions, which include the stops total number, stops' capacity, and the OD matrix. This OD matrix can be updated in this model via a CSV file. Then, we can estimate a new OD matrix for the Intelligent Transport Systems that is supported by the Internet of Things.

Three different parallel architectures (GPUs, FPGAs, and multi-core) were reviewed and analyzed for this work. The main applications for these architectures were described, and the applications related to traffic and public transport simulation were inspected in deep. OpenCL was chosen as the programming framework to implement the new simulation model. Due programs wrote here can be executed across heterogeneous platforms, including the three selected for this work.

Masivo was built with three main components. The first one, the Parameters Loading Module (PLM), which is a Python module that loads the stops information (OD matrix, stops positions, stops max capacity) and the routes information. The second module is the Parallel Simulation Core (PSC), which was built in OpenCL, and that contains the new purposed simulation model. The PCS is designed to run in parallel the operations of each stop, including the passengers' arrival, boarding, and alighting, and to run the buses' displacement process sequentially over the roads. Finally, the Results Statistics Module (RSM) is a Python tool that runs after the PSC to get and analyze the simulation outputs and the performance results.

Furthermore, for Masivo validation, a Pure Python public transport simulator was built for validation purposes. This simulator performed the arrival operations sequentially for each stop. Then, it ran the boarding and alighting operations of each bus that was currently stooped at a station and, finally, executed the buses' update position operations. Furthermore, it had a 3D output graphic interface to visualize the movement of the buses through the different stops, the stops, the bus occupancy, and the alighted passengers at each stop. This visualization tool helped to validate the consistent operations of this simulator and the Masivo PSC. With the Pure Python public transport simulator validated, we used it to validate the Masivo PSC in four different scenarios. We ran each scenario with precisely the same condition in both simulators to compare the simulation output results. The simulation output results for validation consisted of the total alighted passengers per stop and for the whole system, as well as the average commute time per stop and for the whole system. We found that the relative error was no higher than 0.7

% in all the tested scenarios.

The performance of Masivo was evaluated with the speed-up and real-time factor indicators. Masivo achieved a speed-up factor of 10.2 compared with the simulator model running with one compute unit and a speed-up factor of 278 times faster than the Pure Python validation simulator. The real-time factor achieved was 3050 times faster than the 10 h simulated duration. The performance test scenario used consisted of a public transport simulation with 300 stops, 2400 buses, and 456,997 passengers. This performance value was compared with the most recent traffic and public transport model that performed the simulation of systems with similar size. We found that, to date, there are no models reported specifically designed for PTS that can achieve the real-time factor that we have achieved in this research.

Future work with this model could integrate the passengers' interchange between the different public transport modes, such as the train to bus. Furthermore, this model has a fast execution time, making this a high performance solution to use in a public transport optimization resources algorithm.

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Appendix A

Source code

A.1 Masivo PSC OpenCL source code

```
1
2  #ifndef __OPENCL_VERSION__
3  #define __kernel
4  #define __global
5  #define __local
6  #endif
7
8  #define STOP_MAX_PASS   10000
9  #define BUS_MAX_PASS      250
10 #define MAX_STOPS         500
11
12 #define PASS_STATUS_END_LIST    255
13 #define PASS_STATUS_EMPTY         0
14 #define PASS_STATUS_TO_ARRIVE     1
15 #define PASS_STATUS_ARRIVED       2
16 #define PASS_STATUS_IN_BUS        3
17 #define PASS_STATUS_ALIGHTED      4
18
19 #define BUS_TRAVEL_SPEED_M_S          54*1000/3600
20 #define BUS_STOPPING_TIME             20
21
22 #define BUS_NOT_STARTED_STOP  20000
23 #define EMPTY_STOP_NUMBER     20000
24 #define BUS_TRAVELING         20001
25 #define BUS_FINISHED          20002
26
27 #define STOP_BUS_WINDOW_DISTANCE     10
28
29
30 #define FALSE  0
31 #define TRUE   1
32
33 typedef struct {
34   unsigned int    pass_id;
35   unsigned short  orig_stop;
36   unsigned short  dest_stop;
37   unsigned short  arrival_time;
```

```
38    unsigned short  alight_time;
39    unsigned char   status;
40  } __attribute__ ((packed)) PassType;
41
42  // Stop Passengers Struct List (SPSL)
43  typedef struct {
44    unsigned short  stop_num;
45    int             stop_pos;
46    unsigned int    total;
47    unsigned int    last_empty;
48    unsigned int    w_index;
49    PassType        spl[STOP_MAX_PASS];
50  } __attribute__ ((packed)) SpslType;
51
52  // Bus Passengers Struct List (BPSL)
53  typedef struct {
54    unsigned short  number;
55    short           travel_speed_m_s;
56    int             start_pos;
57    unsigned short  last_stop_table_i;
58    int             last_stop_pos;
59    unsigned int    start_time;
60    unsigned short  stops_num_i;
61    short           stop_inc;
62    unsigned short  in_the_stop_counter;
63    unsigned short  in_the_stop;
64    int             curr_pos;
65    unsigned short  curr_stop;
66    unsigned short  last_stop_i;
67    unsigned short  total_stops;
68    unsigned short  stops_num[MAX_STOPS];
69    unsigned int    total;
70    PassType        bpl[BUS_MAX_PASS];
71  } __attribute__ ((packed)) BpslType;
72
73
74  __kernel void masivo_runner(
75    __global SpslType *pwq,               // Passengers Waiting Queue
76    __global SpslType *paq,               // Passengers Arrival Queue
77    __global SpslType *plq,               // Passengers aLight Queue
78    __global BpslType *bpa,               // Bus Passengers Array
79    unsigned int total_stops,                    // Total stops
80    unsigned int total_buses,                    // Total stops
81    unsigned int sim_time
82      )
83  {
84    int gid = get_global_id(0);
85    unsigned int w;
86    char bus_for_dest;
87    unsigned int i,j,k,l,n;
88    char in_the_route;
89    short next_stop_i;
90    unsigned int last_empty_seat_in_bus;
91
92    // bound check (equivalent to the limit on a 'for' loop for standard/serial
          C code
```

```
93    if (gid >= total_stops){
94        return;
95    }
96
97    // *************** PASSENGERS ARRIVING ******************************
98    //printf("In gid %d total: %d\n", gid, pass_arrival_list[gid].total);
99  #if 1
100   //printf("gid: %d, sim_time: %d\n", gid, sim_time);
101   while(TRUE){
102     //printf("pass_id(%d): %d\n", pass_arrival_list[gid].w_index,
103     //pass_arrival_list[gid].spl[pass_arrival_list[gid].w_index].pass_id);
104
105     // Check if the arrival queue is empty
106     if(paq[gid].total == 0){
107       break;
108     }
109
110     w = paq[gid].w_index;
111
112     // Check arrival time
113     if(paq[gid].spl[w].arrival_time > sim_time){
114       break;
115     }
116
117     //printf("In gid %d moving pass_id(%d): %d\n", gid, w, pass_arrival_list[
          gid].spl[w].pass_id);
118     pwq[gid].spl[pwq[gid].last_empty] = paq[gid].spl[w];
119     pwq[gid].spl[pwq[gid].last_empty].status = PASS_STATUS_ARRIVED;
120     pwq[gid].last_empty ++;
121     pwq[gid].total ++;
122
123     paq[gid].spl[w].status = 0;
124     paq[gid].w_index ++;
125     paq[gid].total --;
126
127     //printf("2 pass_id(%d): %d\n", pass_arrival_list[gid].w_index,
128     //pass_arrival_list[gid].spl[pass_arrival_list[gid].w_index].arrival_time
          );
129   }
130 #endif
131
132 #if 1
133   // For each bus
134   for(j = 0; j < total_buses; j++){
135
136     // If the bus is in the stop
137     if(pwq[gid].stop_num == bpa[j].curr_stop){
138
139       // *************** PASSENGERS ALIGHTING
              ******************************
140
141       // Only if there are passengers in the bus
142       if(bpa[j].total > 0){
143
144         // For each passenger in the bus
145         for(k = 0; k < BUS_MAX_PASS; k++){
```

```
146             //printf("pass id to check(%d): %d\n" k, buses_pass_list[j].bpa[k].
                    pass_id)
147
148             // If the passenger status indicate that is the bus
149             if(bpa[j].bpl[k].status == PASS_STATUS_IN_BUS){
150
151               // If the stop is the passsenger destination stop
152               if(bpa[j].bpl[k].dest_stop == pwq[gid].stop_num){
153                 //printf("ALIGHTING pass id %d from bus %d to stop %d\n",
154                 //buses_struc_list[j].bpa[k].pass_id, j, stops_alight_list[gid
                        ].stop_num);
155
156                 // Move the passenger from the bus to the stop alight queue
157                 n = plq[gid].total;
158                 plq[gid].spl[n] = bpa[j].bpl[k];
159                 plq[gid].spl[n].status = PASS_STATUS_ALIGHTED;
160                 plq[gid].spl[n].alight_time = sim_time;
161                 plq[gid].total += 1;
162
163                 bpa[j].bpl[k].status = PASS_STATUS_EMPTY;
164                 bpa[j].total -= 1;
165               }
166             } // End if passger in the bus, if(buses_struc_list[j].bpa[k].
                    status == PASS_STATUS_IN_BUS)
167           }// End For each pass in the bus, for(k = 0; k < BUS_MAX_PASS; k++)
168
169         } // End Only if there are passengers in the bus, if(buses_pass_list[j
                ].total > 0)
170
171         // *************** PASSENGERS BOARDING
                ********************************
172         // If there are not passengers in the stop, do not look for more buses
                to boarding
173         if(pwq[gid].total == 0){
174           break;
175         }
176
177         // If the bus is full, continue with the next bus
178         if(bpa[j].total >= BUS_MAX_PASS){
179           continue;
180         }
181
182         // For this bus, begin the free space search from the beginning
183         last_empty_seat_in_bus = 0;
184         // For each passenger in the stop
185         for(k = 0; k < STOP_MAX_PASS; k++){
186           //printf("Check for board pass_id %d\n", (stops_queue_list[gid].spl[k
                    ].pass_id));
187
188           // If we are at the end of the passenger waiting queue, finish
189           if(pwq[gid].spl[k].status == PASS_STATUS_END_LIST){
190             break;
191           }
192
193           // If the passenger has arrived to the stop
194           if(pwq[gid].spl[k].status == PASS_STATUS_ARRIVED){
```

```
195
196             // Check if the bus route has the passenger destination stop
197             bus_for_dest = FALSE;
198             // For each remaining stops in bus's stop table
199             for(l = bpa[j].last_stop_table_i; l < bpa[j].total_stops; l++){
200               if(pwq[gid].spl[k].dest_stop == bpa[j].stops_num[l]){
201                 bus_for_dest = TRUE;
202                 break;
203               }
204             }
205
206             // If the bus has the destination stop, passenger tryies to board
                    this bus
207             if(bus_for_dest){
208               // Look for a free space in the bus
209               for(n = last_empty_seat_in_bus; n < BUS_MAX_PASS; n++){
210                 //printf("bus seat: %d, status: %d\n",n, buses_struc_list[j].
                        bpa[n].status);
211
212                 // If the seat in the bus is empty
213                 if(bpa[j].bpl[n].status == PASS_STATUS_EMPTY){
214
215                   //printf("BOARDING pass_id %d to the bus %d, in seat %d\n",
216                   //stops_queue_list[gid].spl[k].pass_id, j, n);
217
218                   // Move passenger from stop wating queue to the bus
219                   bpa[j].bpl[n] = pwq[gid].spl[k];
220                   bpa[j].bpl[n].status = PASS_STATUS_IN_BUS;
221                   bpa[j].total += 1;
222
223                   pwq[gid].spl[k].status = PASS_STATUS_EMPTY;
224                   pwq[gid].total -= 1;
225
226                   last_empty_seat_in_bus = n;
227                   break;
228
229                 }
230
231               } // End // Look for a free space in the bus
232
233             } // End If the bus has the destination stop, pass boards  if(
                    bus_for_dest)
234
235           } // End If the pass have arrived to the stop if(pass_list[gid].spl[k
                  ].status == PASS_STATUS_ARRIVED)
236
237         } // End For each pass in the stop for(int k = 0; k < STOP_MAX_PASS; k
                ++)
238
239       } // End If the bus is in the stop
240
241     }// End For each bus for(int j = 0; j < total_buses; j++)
242
243 #endif
244
245
```

```
246   // *************** UPDATE BUSES POSITION ******************************
247 #if 1
248   if(gid == 0){
249     // Update buses
250     // For each bus
251     for(int i = 0; i < total_buses; ++i){
252       // Do not process finished buses
253       if(bpa[i].curr_stop == BUS_FINISHED){
254         continue;
255       }
256 
257       // Check if start the bus
258       if(bpa[i].curr_stop == BUS_NOT_STARTED_STOP){
259         if(sim_time >= bpa[i].start_time){
260           bpa[i].in_the_stop = TRUE;
261           bpa[i].curr_stop = bpa[i].stops_num[0];
262           bpa[i].last_stop_i = bpa[i].stops_num[0];
263           bpa[i].curr_pos = bpa[i].start_pos;
264           bpa[i].last_stop_pos = bpa[i].curr_pos;
265 
266           //printf("Starting bus %d in stop %d start time %d\n",
267           //              buses_struc_list[i].number,
268           //              buses_struc_list[i].curr_stop,
269           //              buses_struc_list[i].start_time);
270         }
271         continue;
272       }
273 
274 
275       // Update bus position
276 
277       // if waiting in the stop
278       //printf("Bus: %d, in_the_stop_flag: %d, curr_stop %d, pos: %d\n",
279       //        buses_struc_list[i].number,
280       //        buses_struc_list[i].in_the_stop,
281       //        buses_struc_list[i].curr_stop,
282       //        buses_struc_list[i].curr_pos);
283 
284       // Check if we have to depart from the stop
285       if(bpa[i].in_the_stop){
286         bpa[i].in_the_stop_counter -= 1;
287         if(bpa[i].in_the_stop_counter == 0){
288           bpa[i].last_stop_table_i += 1;
289           bpa[i].in_the_stop = FALSE;
290           bpa[i].curr_stop = BUS_TRAVELING;
291         }
292       }
293 
294       // if I am not waiting in a stop, go ahead
295       if(bpa[i].curr_stop == BUS_TRAVELING){
296 
297         if(bpa[i].curr_pos > 1000 && bpa[i].curr_pos < 3000){
298           bpa[i].curr_pos += bpa[i].travel_speed_m_s;
299         }else{
300           bpa[i].curr_pos += bpa[i].travel_speed_m_s;
301         }
```

```
302
303
304         }
305
306         // Check if the bus has to leave the current stop, if not, do not check
                for other stop
307         if(abs(bpa[i].last_stop_pos - bpa[i].curr_pos)
308             < STOP_BUS_WINDOW_DISTANCE){
309           continue;
310         }
311
312
313         // Check if the bus is at the next stop
314         next_stop_i = (short)bpa[i].last_stop_i + bpa[i].stop_inc;
315
316         // printf("next_stop_i: %d/%d" % (next_stop_i, buses_struc_list[i].
              total_stops))
317         // Check if the next stop is the last one
318         if((next_stop_i >= bpa[i].total_stops) ||
319           (next_stop_i < 0))
320         {
321           // Finish the bus and put in the rest position
322           bpa[i].curr_stop = BUS_FINISHED;
323           bpa[i].curr_pos = 0;
324           continue;
325         }
326
327         // Look if the bus is inside the stop window of the next stop
328         if(abs(pwq[next_stop_i].stop_pos - bpa[i].curr_pos)
329             < STOP_BUS_WINDOW_DISTANCE){
330
331           // Passing the stop, update last stop index
332           bpa[i].last_stop_i = pwq[next_stop_i].stop_num;
333
334           // Check if the stop is in the routes table to stop thee bus
335           in_the_route = FALSE;
336           for (int j = bpa[i].stops_num_i; j < bpa[i].total_stops; ++j) {
337             if(pwq[next_stop_i].stop_num == bpa[i].stops_num[j]){
338               bpa[i].stops_num_i = j;
339               in_the_route = TRUE;
340             }
341           }
342
343           // if this stop is in the stops table
344           if(in_the_route){
345             //printf("i: %d, Bus %d, in the stop: %d, pos %d\n", i,
346             //  buses_struc_list[i].number,
347             //  stops_queue_list[next_stop_i].stop_num,
348             //  buses_struc_list[i].curr_pos);
349
350             bpa[i].curr_stop = pwq[next_stop_i].stop_num;
351             bpa[i].last_stop_pos = pwq[next_stop_i].stop_pos;
352             bpa[i].in_the_stop = TRUE;
353             bpa[i].in_the_stop_counter = BUS_STOPPING_TIME;
354           }
355         }
```

```
356
357       } // End for each bus for(int i = 0; i < total_buses; ++i){
358
359     } // End if(gid == 0){
360
361   #endif
362   }
```

Appendix B

Validation simulator other results

B.1 Results for 30 stops, normal distribution ODM

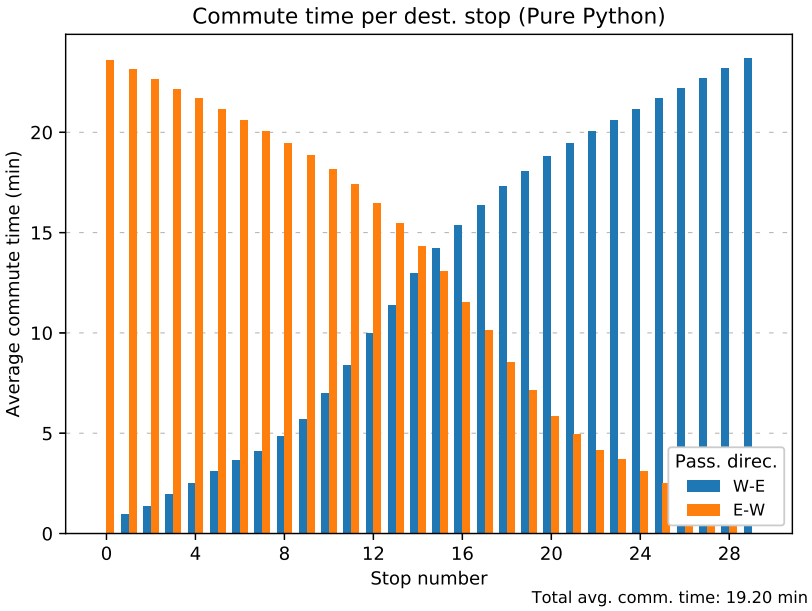

Figure B.1: Commute time per stop for 30 stops normal distribution ODM

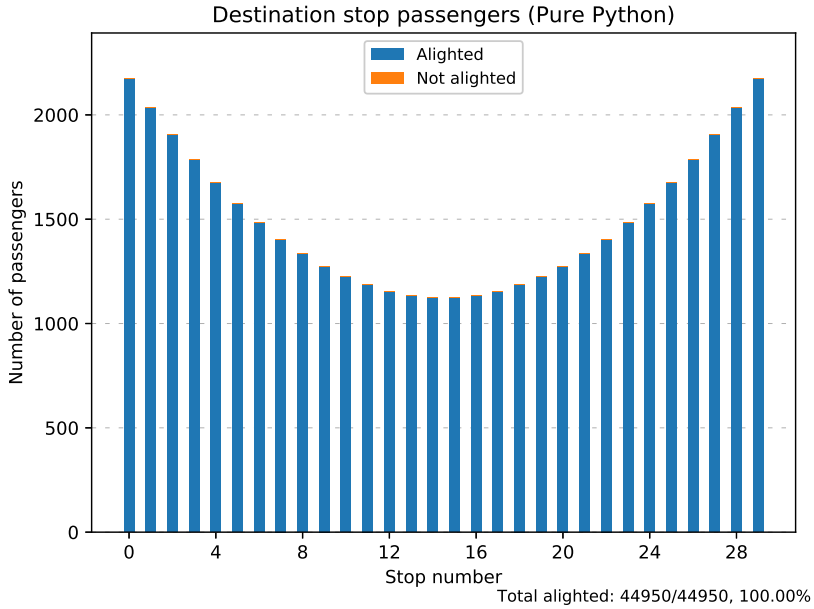

Figure B.2: Alighted passengers per stop, for 30 stops normal distribution ODM

B.2 Results for 30 stops, with downtown in stops 16 to 22

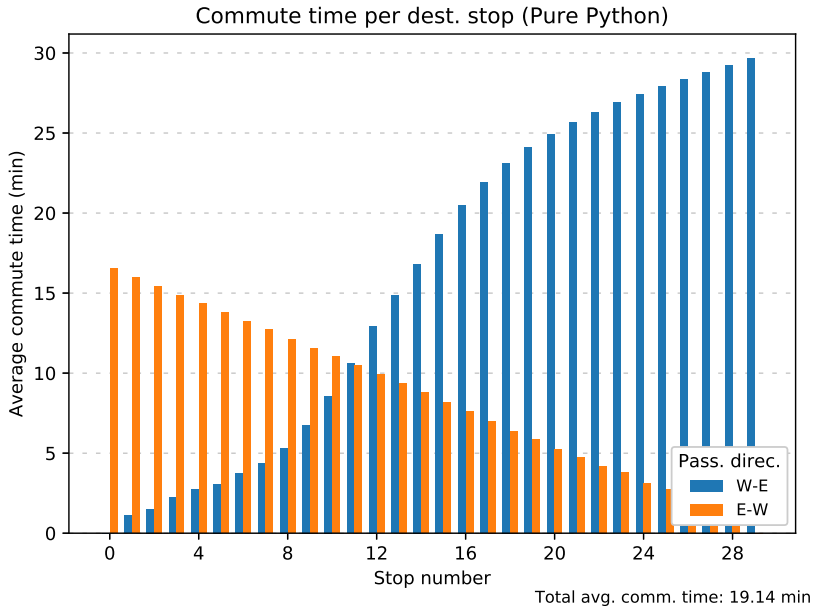

Figure B.3: Commute time per stop for 30 stops with downtown in stops 16 to 22

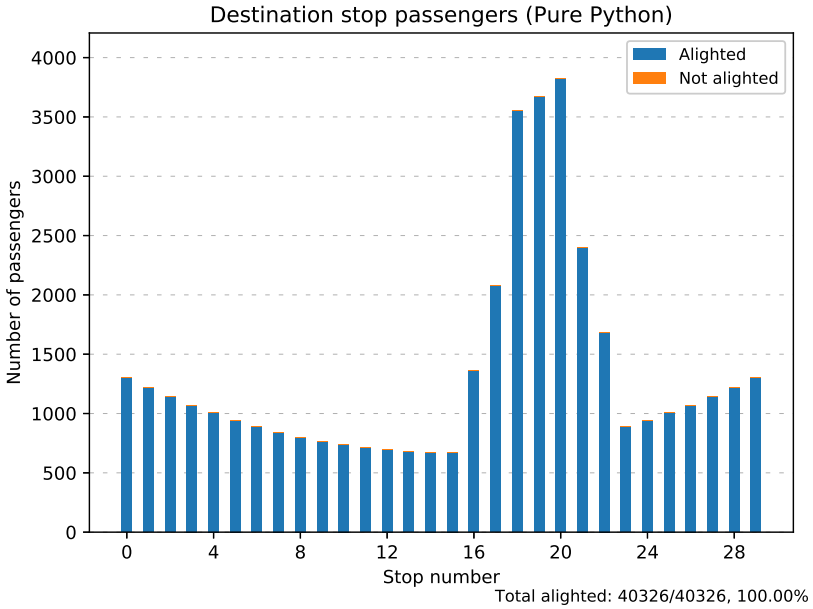

Figure B.4: Alighted passengers per stop, for 30 stops with downtown in stops 16 to 22

B.3 Results for 30 stops, with downtown and random passengers

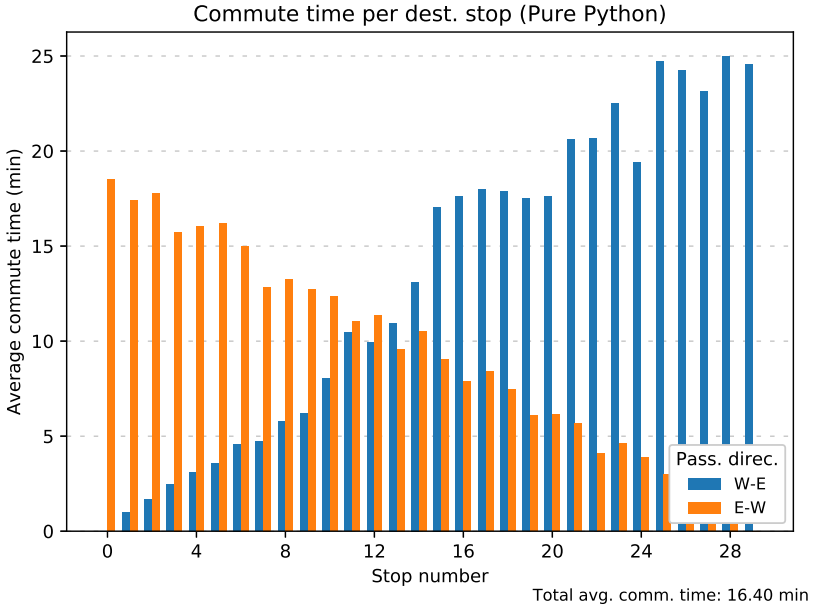

Figure B.5: Commute time per stop for 30 stops with downtown and random passengers

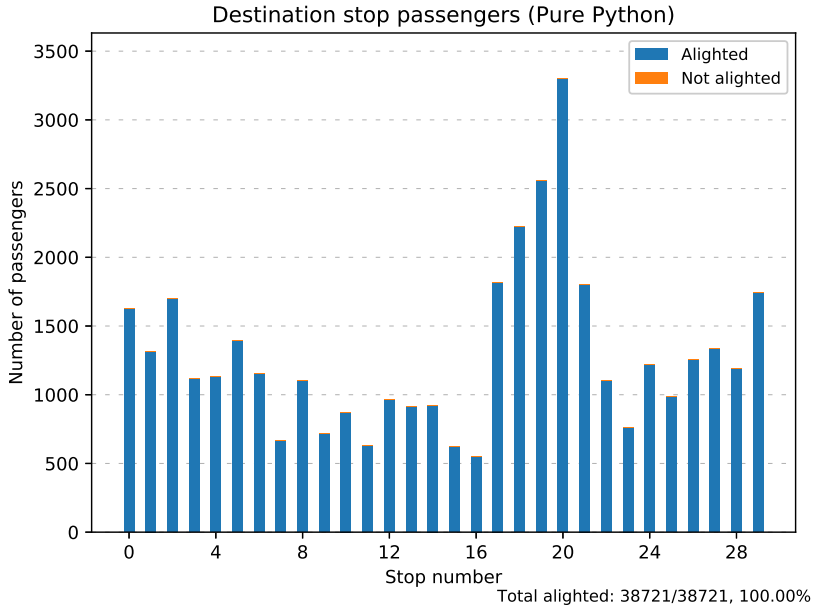

Figure B.6: Alighted passengers per stop, for 30 stops with downtown and random passengers

B.4 Results for 300 stops, with corners high demand and random passengers

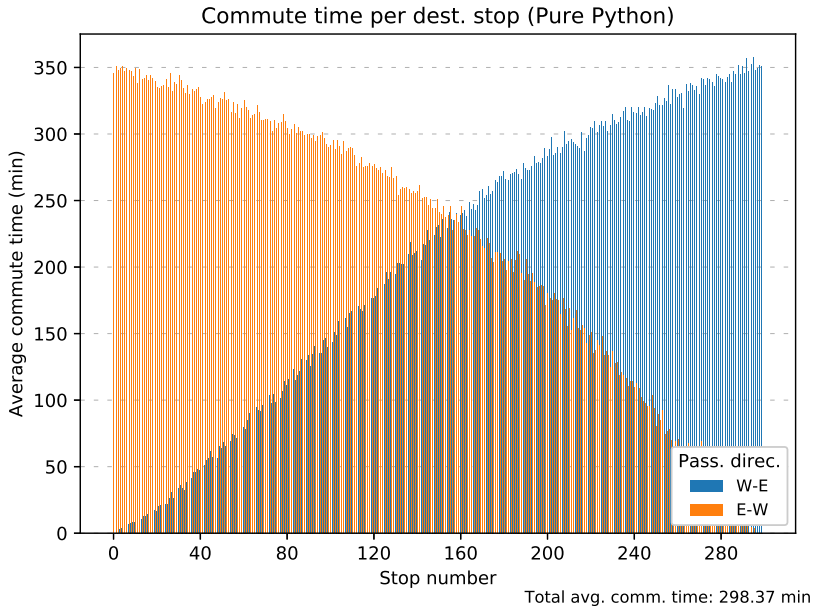

Figure B.7: Commute time per stop for stops, with corners high demand and random passengers

B.4. Results for 300 stops, with corners high demand and random passengers

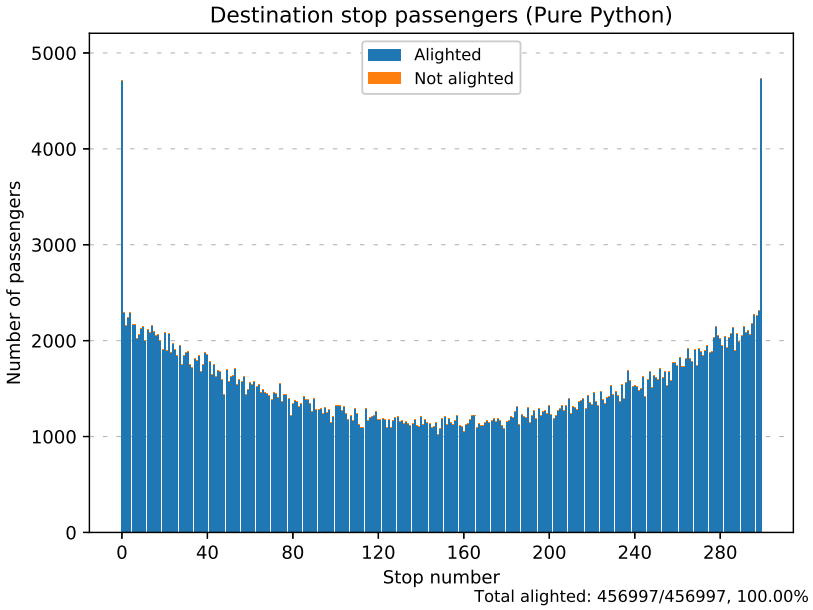

Figure B.8: Alighted passengers per stop, for stops, with corners high demand and random passengers