ARQUITECTURA DE LA PLATAFORMA TECNOLÓGICA DEL SISTEMA DE BICICLETAS COMPARTIDAS PARA LA CIUDAD DE POPAYÁN.

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Departamento de Telecomunicaciones
Popayán, 2017.

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Trabajo de Grado presentado como requisito para obtener el título de Ingeniero en Electrónica y Telecomunicaciones

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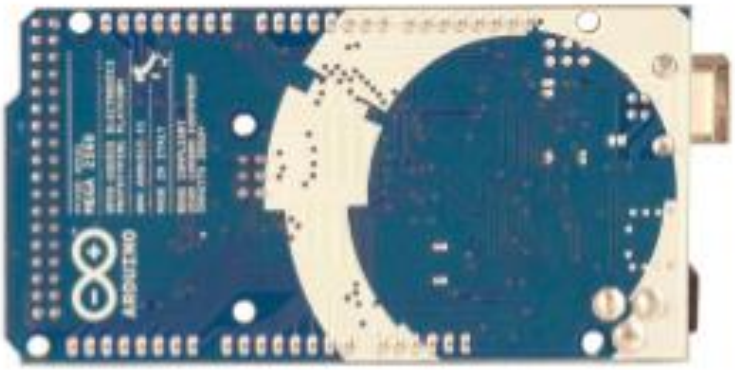
ANEXO A: DATASHEET ARDUINO MEGA256

Arduino Mega 2560



Overview

The Arduino Mega 2560 is a microcontroller board based on the ATmega2560 (datasheet). It has 54 digital input/output pins (of which 14 can be used as PWM outputs), 16 analog inputs, 4 UARTs (hardware serial ports), a 16 MHz crystal oscillator, a USB connection, a power jack, an ICSP header, and a reset button. It contains everything needed to support the microcontroller; simply connect it to a computer with a USB cable or power it with a AC-to-DC adapter or battery to get started. The Mega is compatible with most shields designed for the Arduino Duemilanove or Diecimila.

Schematic & Reference Design

EAGLE files: arduino-mega2560-reference-

design.zip Schematic: arduino-mega2560-

schematic.pdf

Summary

Microcontroller	ATmega2560
Operating Voltage	5V Input Voltage (recommended) 7-12V Input Voltage (limits) 6-20V
Digital I/O Pins	54 (of which 14 provide PWM output)
Analog Input Pins	16
DC Current per I/O Pin	40 mA DC Current for 3.3V Pin 50 mA
Flash Memory	256 KB of which 8 KB used by bootloader
SRAM	8 KB
EEPROM	4 KB
Clock Speed	16 MHz

Power

The Arduino Mega can be powered via the USB connection or with an external power supply. The power source is selected automatically.

External (non-USB) power can come either from an AC-to-DC adapter (wall-wart) or battery. The adapter can be connected by plugging a 2.1mm center-positive plug into the board's power jack. Leads from a battery can be inserted in the Gnd and Vin pin headers of the POWER connector.

The board can operate on an external supply of 6 to 20 volts. If supplied with less than 7V, however, the 5V pin may supply less than five volts and the board may be unstable. If using more than 12V, the voltage regulator may overheat and damage the board. The recommended range is 7 to 12 volts.

The Mega2560 differs from all preceding boards in that it does not use the FTDI USB-to-serial driver chip. Instead, it features the Atmega8U2 programmed as a USB-to-serial converter.

The power pins are as follows:

-VIN. The input voltage to the Arduino board when it's using an external power source (as opposed to 5 volts from the USB connection or other regulated power source). You can supply voltage through this pin, or, if supplying voltage via the power jack, access it through this pin.

-5V. The regulated power supply used to power the microcontroller and other components on the board. This can come either from VIN via an on-board regulator, or be supplied by USB or another regulated 5V supply.

-3V3. A 3.3 volt supply generated by the on-board regulator. Maximum current draw is 50 mA.

-GND. Ground pins.

Memory

The ATmega2560 has 256 KB of flash memory for storing code (of which 8 KB is used for the bootloader), 8 KB of SRAM and 4 KB of EEPROM (which can be read and written with the EEPROM library).

Input and Output

Each of the 54 digital pins on the Mega can be used as an input or output, using pinMode(), digitalWrite(), and digitalRead() functions. They operate at 5 volts. Each pin can provide or receive a maximum of 40 mA and has an internal pull-up resistor (disconnected by default) of 20-50 kOhms. In addition, some pins have specialized functions:

-Serial: 0 (RX) and 1 (TX); Serial 1: 19 (RX) and 18 (TX); Serial 2: 17 (RX) and 16 (TX); Serial 3: 15 (RX) and 14 (TX). Used to receive (RX) and transmit (TX) TTL serial data. Pins 0 and 1 are also connected to the corresponding pins of the ATmega8U2 USB-to-TTL Serial chip.

-External Interrupts: 2 (interrupt 0), 3 (interrupt 1), 18 (interrupt 5), 19 (interrupt 4), 20 (interrupt 3), and 21 (interrupt 2). These pins can be configured to trigger an interrupt on a low value, a rising or falling edge, or a change in value. See the attachInterrupt() function for details.

-PWM: 0 to 13. Provide 8-bit PWM output with the analogWrite() function.

-SPI: 50 (MISO), 51 (MOSI), 52 (SCK), 53 (SS). These pins support SPI communication using the SPI library. The SPI pins are also broken out on the ICSP header, which is physically compatible with the Uno, Duemilanove and Diecimila.

-LED: 13. There is a built-in LED connected to digital pin 13. When the pin is HIGH value, the LED is on, when the pin is LOW, it's off.

-I2C: 20 (SDA) and 21 (SCL). Support I2C (TWI) communication using the Wire library (documentation on the Wiring website). Note that these pins are not in the same location as the I2C pins on the Duemilanove or Diecimila.

The Mega2560 has 16 analog inputs, each of which provide 10 bits of resolution (i.e. 1024 different values). By default they measure from ground to 5 volts, though is it possible to change the upper end of their range using the AREF pin and analogReference() function.

There are a couple of other pins on the board:

-AREF. Reference voltage for the analog inputs. Used with analogReference().

-Reset. Bring this line LOW to reset the microcontroller. Typically used to add a reset button to shields which block the one on the board.

Communication

The Arduino Mega2560 has a number of facilities for communicating with a computer, another Arduino, or other microcontrollers. The ATmega2560 provides four hardware UARTs for TTL (5V) serial communication. An ATmega8U2 on the board channels one of these over USB and provides a virtual com port to software on the computer (Windows machines will need a .inf file, but OSX and Linux machines will recognize the board as a COM port automatically. The Arduino software includes a serial monitor which allows simple textual data to be sent to and from the board. The RX and TX LEDs on the board will flash when data is being transmitted via the ATmega8U2 chip and USB connection to the computer (but not for serial communication on pins 0 and 1).

A SoftwareSerial library allows for serial communication on any of the Mega2560's digital pins.

The ATmega2560 also supports I2C (TWI) and SPI communication. The Arduino software includes a Wire library to simplify use of the I2C bus; see the documentation on the Wiring website for details. For SPI communication, use the SPI library.

Programming

The Arduino Mega can be programmed with the Arduino software (download). For details, see the reference and tutorials.

The ATmega2560 on the Arduino Mega comes preburned with a bootloader that allows you to upload new code to it without the use of an external hardware programmer. It communicates using the original STK500 protocol (reference, C header files).

You can also bypass the bootloader and program the microcontroller through the ICSP (In-Circuit Serial Programming) header; see these instructions for details.

The ATmega8U2 firmware source code is available in the Arduino repository. The ATmega8U2 is loaded with a DFU bootloader, which can be activated by connecting the solder jumper on the back of the board (near the map

of Italy) and then resetting the 8U2. You can then use Atmel's FLIP software (Windows) or the DFU programmer (Mac OS X and Linux) to load a new firmware. Or you can use the ISP header with an external programmer (overwriting the DFU bootloader). See this user-contributed tutorial for more information.

Automatic (Software) Reset

Rather then requiring a physical press of the reset button before an upload, the Arduino Mega2560 is designed in a way that allows it to be reset by software running on a connected computer. One of the hardware flow control lines (DTR) of the ATmega8U2 is connected to the reset line of the ATmega2560 via a 100 nanofarad capacitor. When this line is asserted (taken low), the reset line drops long enough to reset the chip. The Arduino software uses this capability to allow you to upload code by simply pressing the upload button in the Arduino environment. This means that the bootloader can

have a shorter timeout, as the lowering of DTR can be well-coordinated with the start of the upload.

This setup has other implications. When the Mega2560 is connected to either a computer running Mac OS X or Linux, it resets each time a connection is made to it from software (via USB). For the following half-second or so, the bootloader is running on the Mega2560. While it is programmed to ignore malformed data (i.e. anything besides an upload of new code), it will intercept the first few bytes of data sent to the board after a connection is opened. If a sketch running on the board receives one-time configuration or other data when it first starts, make sure that the software with which it communicates waits a second after opening the connection and before sending this data.

The Mega2560 contains a trace that can be cut to disable the auto-reset. The pads on either side of the trace can be soldered together to re-enable it. It's labeled "RESET-EN". You may also be able to disable the auto-reset by connecting a 110 ohm resistor from 5V to the reset line; see this forum thread for details.

USB Overcurrent Protection

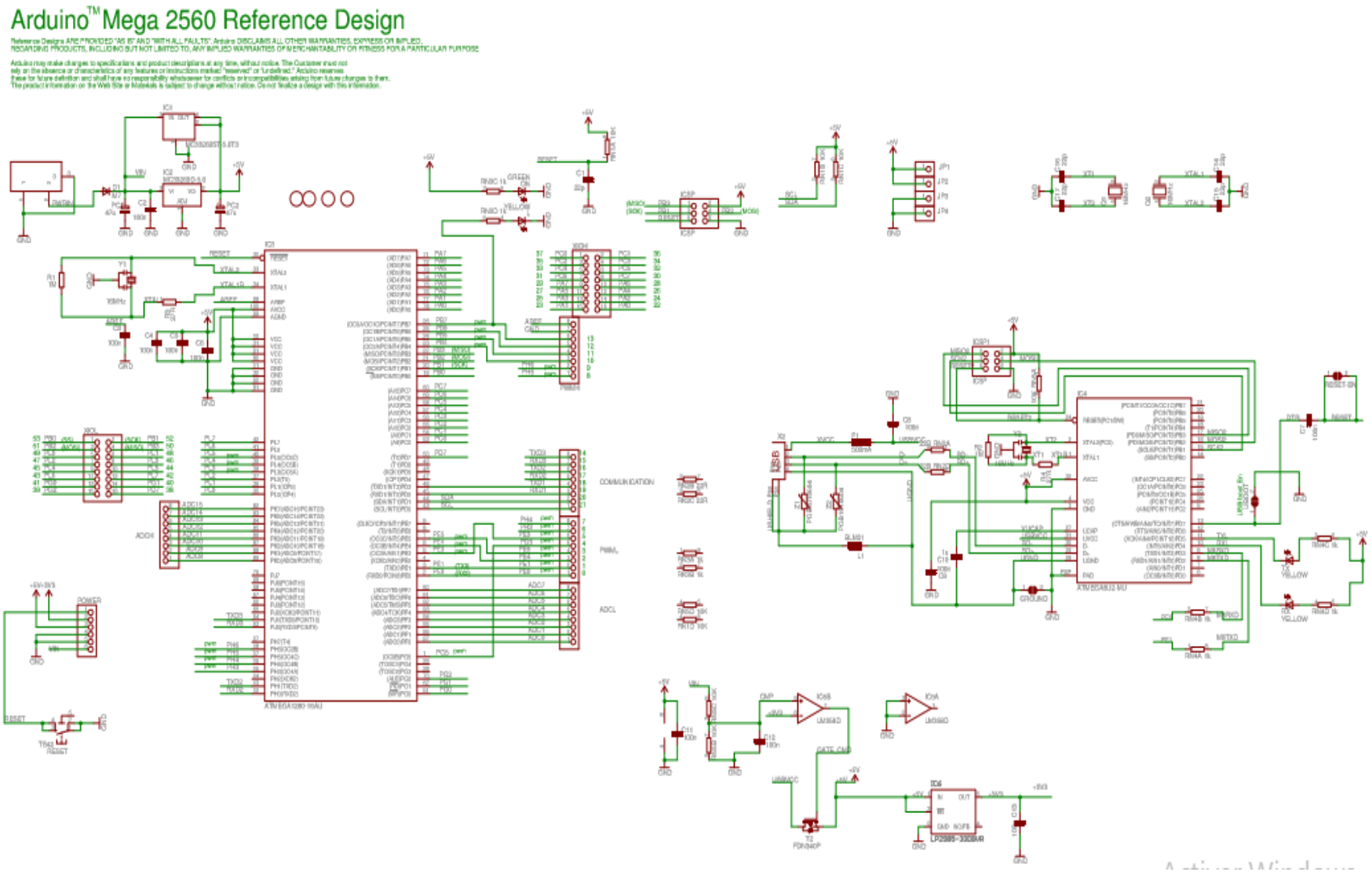
The Arduino Mega2560 has a resettable polyfuse that protects your computer's USB ports from shorts and overcurrent. Although most computers provide their own internal protection, the fuse provides an extra layer of protection. If more than 500 mA is applied to the USB port, the fuse will automatically break the connection until the short or overload is removed.

Physical Characteristics and Shield Compatibility

The maximum length and width of the Mega2560 PCB are 4 and 2.1 inches respectively, with the USB connector and power jack extending beyond the former dimension. Three screw holes allow the board to be attached to a surface or case. Note that the distance between digital pins 7 and 8 is 160 mil (0.16"), not an even multiple of the 100 mil spacing of the other pins.

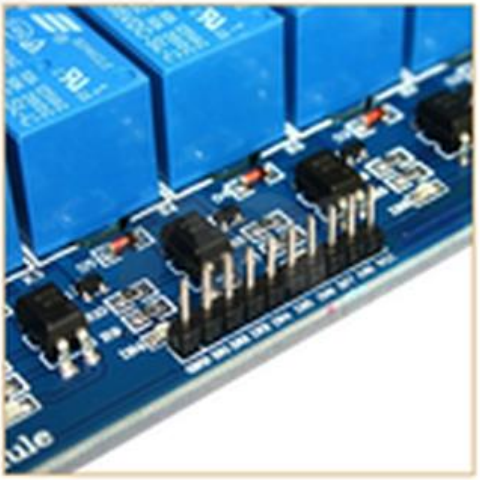
The Mega2560 is designed to be compatible with most shields designed for the Uno, Diecimila or Duemilanove. Digital pins 0 to 13 (and the adjacent AREF and GND pins), analog inputs 0 to 5, the power header, and ICSP header are all in equivalent locations. Further the main UART (serial port) is located on the same pins (0 and 1), as are external interrupts 0 and 1 (pins 2 and 3 respectively). SPI is available through the ICSP header on both the Mega2560 and

Duemilanove / Diecimila. *Please note that I^2C is not located on the same pins on the Mega (20 and 21) as the Duemilanove / Diecimila (analog inputs 4 and 5)*


Arduino™ Mega 2560 Reference Design

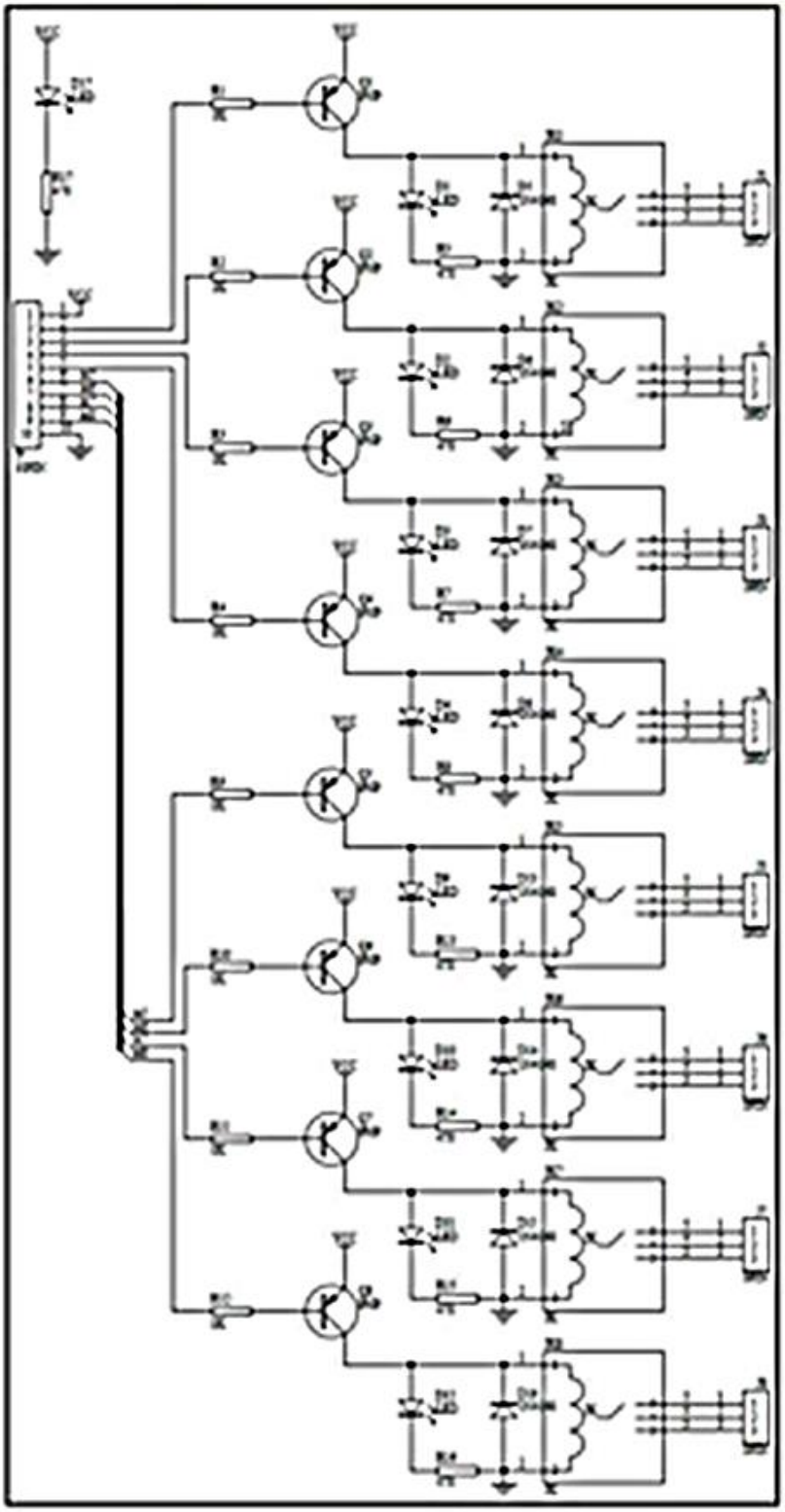
ANEXO B: DATASHEET MODULO RELE OPTOCOPLADO

MODULO RELES 8CH OPTO-AISLADOS 5Vdc



Caracteristicas:

- 8 Canales de reles NC/NA (250Vac-10A/30Vdc-10A)
- Opto-Aislación (De esta manera protejes tu etapa de control)
- Entrada : 5 Vdc -15 a 20 ma (Led indicador de control)
- Interface estandar para multiples aplicaciones (PIC-AVR-ARM-DSP-ARDUINO)
- Medidas : 13.9cm x 5.2cm x 1.7cm



ANEXO C: DATASHEET MODULO CC3000.

FEATURES

- **Wireless network processor**
  - **IEEE 802.11 b/g**
  - **Embedded IPv4 TCP/IP stack**
- **Best-in-class radio performance**
  - **TX power: +18.0 dBm at 11 Mbps, CCK**
- **Operating temperature: –20°C to 70°C**
- **Based on TI's seventh generation of proven Wi-Fi solutions**
- **Complete platform solution including user and porting guides, API guide, sample applications, and support community**

DESCRIPTION

The TI CC3000 module is a self-contained wireless network processor that simplifies the implementation of Internet connectivity (see Figure 1). TI's SimpleLink™ Wi-Fi solution minimizes the software requirements of the host microcontroller (MCU) and is thus the ideal solution for embedded applications using any low-cost and low- power MCU.

The TI CC3000 module reduces development time, lowers manufacturing costs, saves board space, eases certification, and minimizes the RF expertise required. This complete platform solution includes software drivers, sample applications, API guide, user documentation, and a world-class support community.

For more information on TI's wireless platform solutions for Wi-Fi, go to TI's Wireless Connectivity wiki (www.ti.com/connectivitywiki).

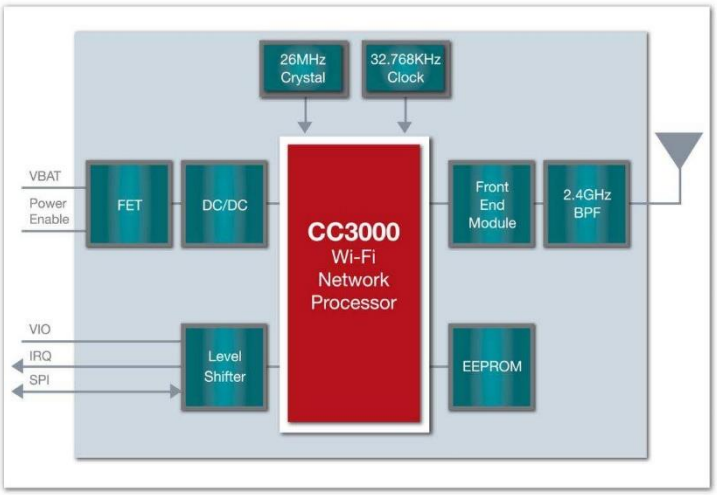


Figure 1. Wi-Fi Solution for TI SimpleLink CC3000 Module

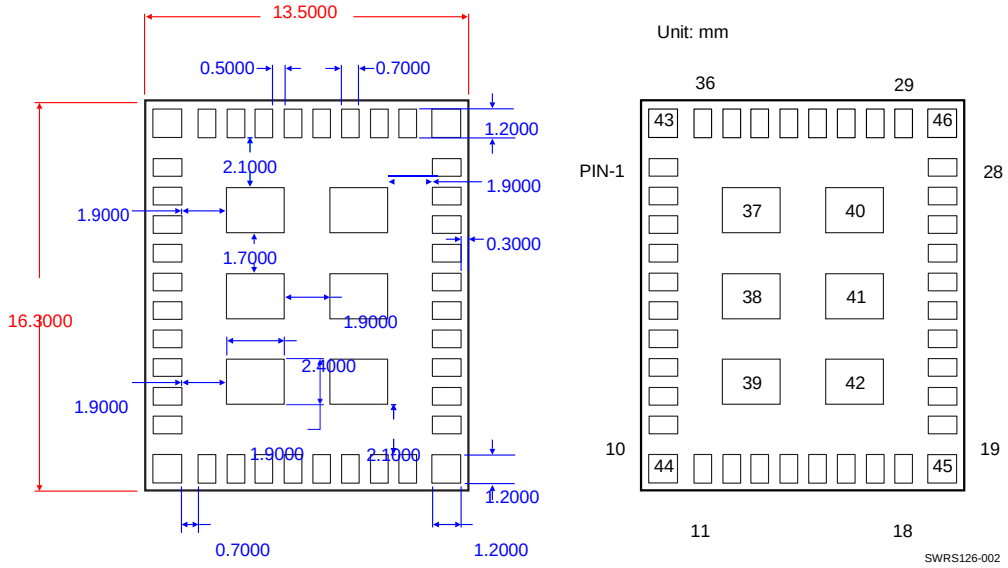
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SimpleLink, Smart Config are trademarks of Texas Instruments. Wi-Fi is a trademark of Wi-Fi Alliance.

PACKAGE INFORMATION

Module Outline

For the PCB layout of your applications, TI recommends the footprint shown in Figure 2.



Pin Description

Table 1 describes the CC3000 module pins.

Table 1. CC3000 Module Pins Description

Pin	Signal Name	Type	State at Reset	State After Reset	Voltage Level	Description
1	GND	GND	—	—	—	Ground
2	Reserved_1	—	—	—	1.8 V	Reserved. Connect to test point.
3	NC	—	—	—	—	Not connected
4	Reserved_2	—	—	—	1.8 V	Reserved. Connect to test point.
5	WL_EN2(1)	I	Hi-Z	—	—	Mode setting
6	WL_RS232_TX(2)	O	Hi-Z	Force 1	1.8 V	RS232 test-mode signal (1.8-V logic). Connect to test point. Serial connection for CC3000 radio tool.
7	WL_EN1	I	Hi-Z	—	—	Mode setting
8	WL_RS232_RX(2)	I	Hi-Z	PU	1.8 V	RS232 test-mode signal (1.8-V logic). Connect to test point. Serial connection for CC3000 radio tool.
9	GND	GND	—	—	—	Ground
10	GND	GND	—	—	—	Ground
11	GND	GND	—	—	—	Ground
12	SPI_CS	I	Hi-Z	PU	VIO_HOST	Host interface SPI chip-select (CS)
13	SPI_DOUT	O	Hi-Z	PU	VIO_HOST	Host interface SPI data out
14	SPI_IRQ	O	Hi-Z	Force 1	VIO_HOST	Host interface SPI interrupt

(1) Connect WL_EN1 to WL_EL2 for proper operation of the module.
(2) Leave unconnected in function module.

Table 1. CC3000 Module Pins Description (continued)

Pin	Signal Name	Type	State at Reset	State After Reset	Voltage Level	Description
15	SPI_DIN	I	Hi-Z	PU	VIO_HOST	Host interface SPI data in
16	GND	GND	—	—	—	Ground
17	SPI_CLK	I	Hi-Z	PD	VIO_HOST	Host interface SPI clock
18	GND	GND	—	—	—	Ground
19	VBAT_IN	Power	—	—	V_{BAT}	Power supply input, 2.7 to 4.8 V
20	GND	GND	—	—	—	Ground
21	EXT_32K	—	—	—	—	Not used. Connect to ground.
22	GND	GND	—	—	—	Ground
23	VIO_HOST	Power	—	—	VIO_HOST	VIO host supply voltage
24	Reserved 3	—	—	—	—	Reserved. Connect to test point.
25	GND	GND	—	—	—	Ground
26	VBAT_SW_EN	I	—	—	VIO_HOST	Module enable. Connect to host GPIO.
27	SDA_EEPROM(3)	I/O			1.8 V	I2C data line from EEPROM
28	SDA_CC3000(3)	I/O			1.8 V	I2C data line from the CC3000 module
29	SCL_EEPROM(4)	I/O			1.8 V	I2C clock line from EEPROM
30	SCL_CC3000(4)	I/O			1.8 V	I2C clock line from the CC3000 module
31	GND	GND	—	—	—	Ground
32	GND	GND	—	—	—	Ground
33	GND	GND	—	—	—	Ground
34	GND	GND	—	—	—	Ground
35	RF_ANT	RF	—	—	—	WLAN antenna port, 50-Ω single
36	GND	GND	—	—	—	Ground
37	GND	GND	—	—	—	Ground
38	GND	GND	—	—	—	Ground
39	GND	GND	—	—	—	Ground
40	GND	GND	—	—	—	Ground
41	GND	GND	—	—	—	Ground
42	GND	GND	—	—	—	Ground
43	GND	GND	—	—	—	Ground
44	GND	GND	—	—	—	Ground
45	GND	GND	—	—	—	Ground
46	GND	GND	—	—	—	Ground

(1) Connect SDA_EEPROM and SDA_CC3000 through a 0-Ω resistor.
(2) Connect SLC_EEPROM and SLC_CC3000 through a 0-Ω resistor.

ESD PERFORMANCE

Because electrostatic discharge (ESD) can damage this integrated circuit, TI recommends handling all integrated circuits (ICs) with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision ICs can be more susceptible to damage because very small parametric changes can cause devices not to meet their published specifications.

Table 2 describes the ESD performance.

Table 2. ESD Performance

HDM(1)	CDM(2)
1000 V	500 V

(1) JEDEC ESD HBM spec JS-001-2012
(2) JEDEC ESD CDM spec 22C101E

MODULE SPECIFICATIONS

Absolute Maximum Ratings

Parameters	Pin	Min	Max	Unit
VBAT_IN	19	–0.5	+6.0	V
VIO_HOST	23	–0.5	+4.6	V
I2C and WL_RS232	27, 28, 29, 30, 6, 8	–0.5	+2.1	V
SPI interface	12, 13, 14, 15, 17	–0.5	+4.6	V
VBAT_SW_EN	26	–0.3	+6.0	V
Storage temperature range	–	–40	+85	°C

Recommended Operating Conditions

Rating	Condition		Sym	Min	Max	Unit
Operating ambient temperature				–20	+70	°C
VBAT_IN				2.7	4.8	V
VIO_HOST supply voltage				1.8	3.6	V
SPI interface						
High-level input voltage	VIO_HOST =	1.8 to 1.95 V	VIH	VIO_HOST x 0.65		V
		1.95 to 2.7 V		1.6		
		2.7 to 3.6 V		2		
Low-level input voltage	VIO_HOST =	1.8 to 1.95 V	VIL		VIO_HOST × 0.35	V
		1.95 to 2.7 V			0.7	
		2.7 to 3.6 V			0.8	
Input voltage			VI	0	3.6	V
Output voltage	Active state		VO	0	VIO_HOST	V
Input transition rise or fall rate			△t/△v		5	ns/V
VBAT SW EN						
High-level input voltage			VIH	1.1	5.5	V
Low-level input voltage			VIL	0	0.4	V

Power Consumption

Parameters	Test Conditions	Typ	Max	Unit
802.11b TX current	VBAT = 3.6 V Tamb = +25°C Po = 18 dBm, 11 Mbps L = 2048 bytes tdelay (idle) = 40 µs	260	275	mA
802.11g TX current	VBAT = 3.6 V Tamb = +25°C Po = 14 dBm, 54 Mbps L = 2048 tdelay (idle) = 40 µs	190	207	mA
802.11bg RX current	VBAT = 3.6 V	92	103	mA
Shut-down mode	VBAT = 3.6 V VBAT_SW_EN = 0 V		5	µA

WLAN Transmitter RF Characteristics

(TA = +25°C, VBAT = 3.6 V)

Characteristics	Condition (Mbps)	Min	Typ	Max	Unit
Maximum RMS output power	1		18.3		dBm
	2		18.2		
	11		18.1		
	6		17.0		
	9		17.0		
	18		17.0		
	36		15.5		
	54		14.0		
In-band power variation				±1	
Transmit center frequency accuracy				±20	ppm

Receiver RF Characteristics

(TA = +25°C, VBAT = 3.6 V)

Characteristics	Condition (Mbps)	Min	Typ	Max	Unit
Sensitivity	1 DSSS		–97.5		dBm
	2 DSSS		–95.0		
	11 CCK		–89.0		
	6 OFDM		–91.0		
	9 OFDM		–91.0		
	18 OFDM		–87.0		
	36 OFDM		–81.0		
	54 OFDM		–75.0		
Maximum input level	802.11b			–10	dBm
	802.11g			–20	

SPI HOST CONTROLLER INTERFACE

The SPI is the primary host interface to the CC3000 module.

The SPI interface contains the five-line, master and slave communication model shown in Figure 3.

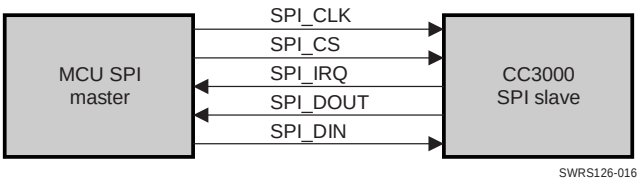


Figure 3. SPI Host Connectivity

Table 3 highlights the CC3000 SPI pin names and functions.

Table 3. SPI Line Description

Pin Name	Description
SPI_CLK	Clock (0 to 16 MHz) from host to slave
SPI_CS(1)	CS (active low) signal from host to slave
SPI_DIN	Data from host to slave
SPI_IRQ(2)	Interrupt from slave to host
SPI_DOUT	Data from slave to host

(1) SPI_CS selects a CC3000 module, indicating that a master wants to communicate to the device.
(2) SPI_IRQ is a dual-purpose slave to the master direction line: in SPI IDLE state while no data transfer is active, driving SPI_IRQ low indicates to the master that the CC3000 module has data to pass to it; driving SPI_IRQ low following SPI_CS deassertion indicates that the CC3000 module is ready to receive data.

SPI Timing

Figure 4 shows the SPI timing sequence.

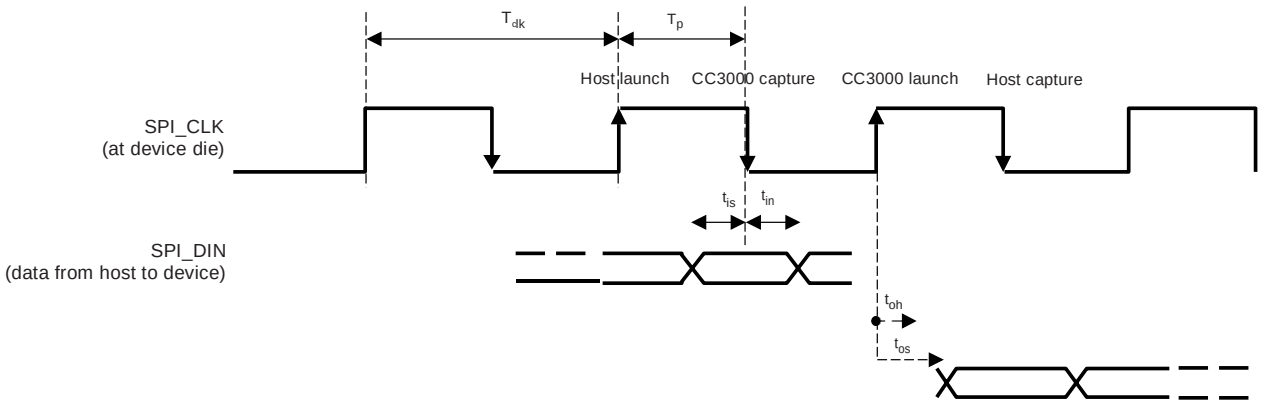


Table 4 lists the SPI timing parameters.

Table 4. SPI Timing Parameters

Symbol	Parameter(1)(2)	Min	Max	Unit
T_{clk}	Clock period	62.5		ns
T_p	High pulse width (including jitter and duty cycle)	25(3)	37.5(3)	ns
t_{is}	RX setup time; minimum time in which data is stable before capture edge	5		ns
t_{ih}	RX hold time; minimum time in which data is stable after capture edge	5		
t_{os}	TX setup propagation time; maximum time from launch edge until data is stable		10.2	
t_{oh}	TX hold propagation time; minimum time of data stable after launch edge	3		
C_L	Capacitive load on interface		20	pF

(1) The SPI_CS signal is considered to be asynchronous.
(2) In this example, launch is on the rising edge, and capture is on the falling edge. The opposite scheme can be configured.
(3) 40% to 60% DC (valid for the minimum clock period)

POWER-UP SEQUENCE

Figure 5 demonstrates the wake-up sequence of the CC3000 module.

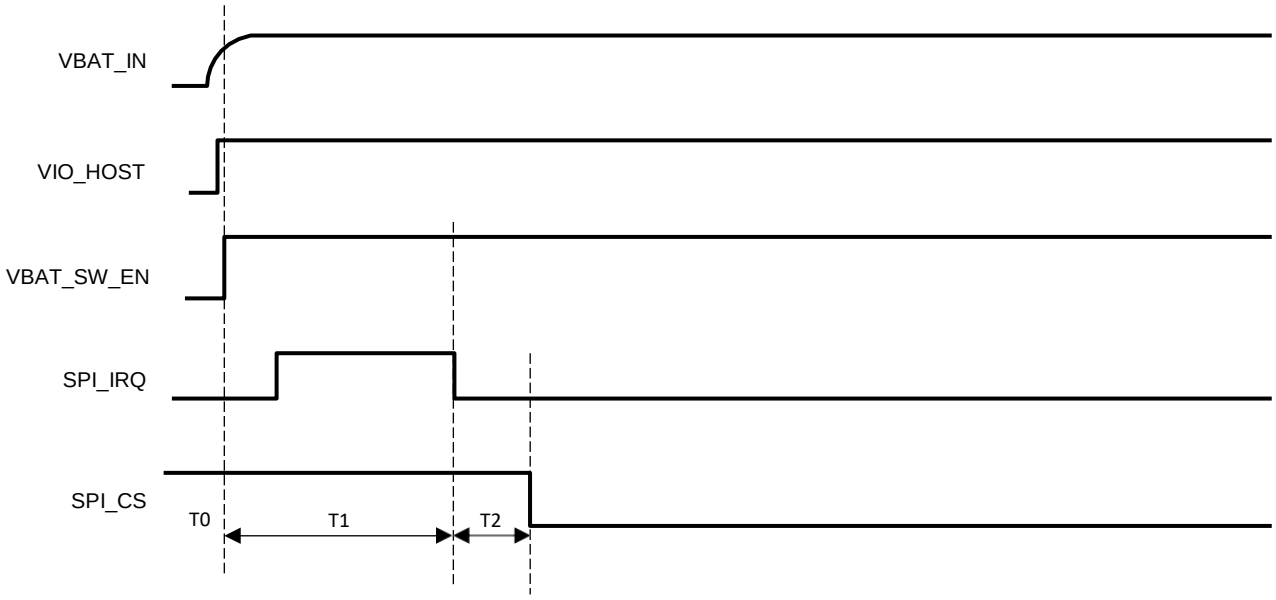


Figure 5. CC3000 Module Power-On Sequences

NOTE

- VBAT_IN and VIO_HOST must be available before VBAT_SW_EN is asserted.
- At wake-up time (T1): The CC3000 module powers up after SPI_IRQ changes state to LOW. T1 is approximately 53 ms.
- At T2: The normal master SPI write sequence is SPI_CS low, followed by SPI_IRQ low (CC3000 host), indicating that the CC3000 core module is ready to accept data. T2 duration is approximately 7 ms.

CC3000 Enable Pins Configuration

Table 5 describes the CC3000 mode of operation based on the enable (EN) pins setting.

Table 5. CC3000 EN Pins Configuration

Mode	State
Test mode(1)	WL_EN1: Leave disconnected. WL_EN2: Connect to ground.
Functional mode(2)	WL_EN1 and WL_EN2 are shorted together.

(1) For CC3000 radio tool operation
(2) For normal operation

Test Mode Serial Interface

The CC3000 module contains a dedicated WLAN serial interface to connect to the CC3000 radio tests tool, an external PC-based software test utility, during development and evaluation phase (see Figure 6 and Table 6). The CC3000 radio test tool utility can be obtained from the CC3000 TI wiki (www.ti.com/connectivitywiki).

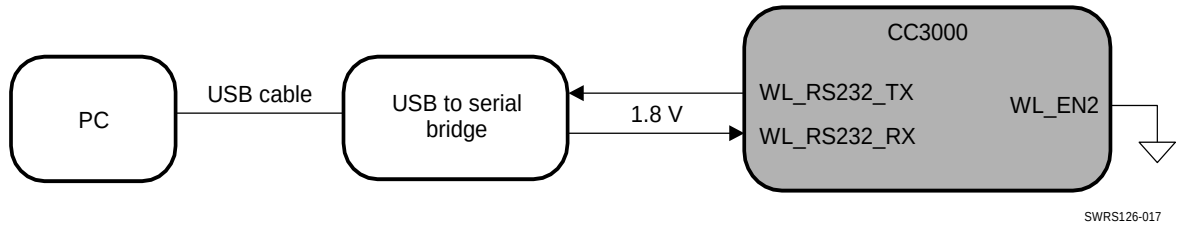


Figure 6. CC3000 Test Mode Serial Interface Connection

Signal Name	Function
WL_RS232_TX	Connection with CC3000 radio PC-based software(1)
WL_RS232_RX	

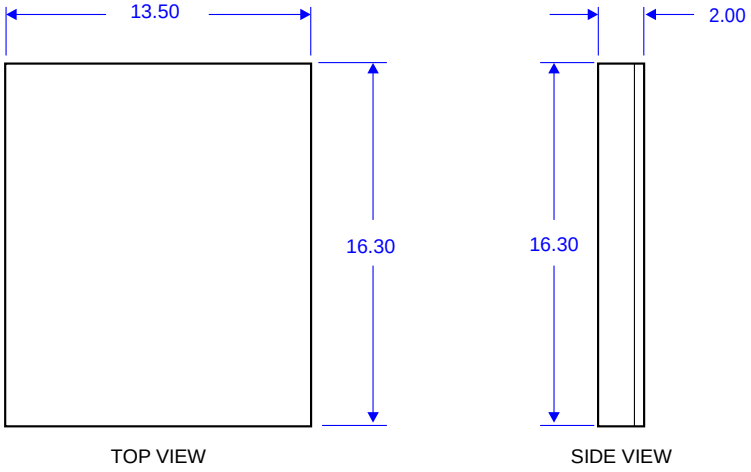
SURFACE MOUNT INFORMATION

The CC3000 module uses a flat shield cover designed for a fully automated assembly process. For baking and reflow recommendations, follow MSL level 4 found in the JEDEC/IPC Standard J-STD-20b. The classification temperature (T_C) for the module is 250°C.

MECHANICAL INFORMATION

Module Mechanical Outline

Figure 7 shows the mechanical outline for the CC3000 module.



Package Marking

Figure 8 shows the CC3000 module package marking.

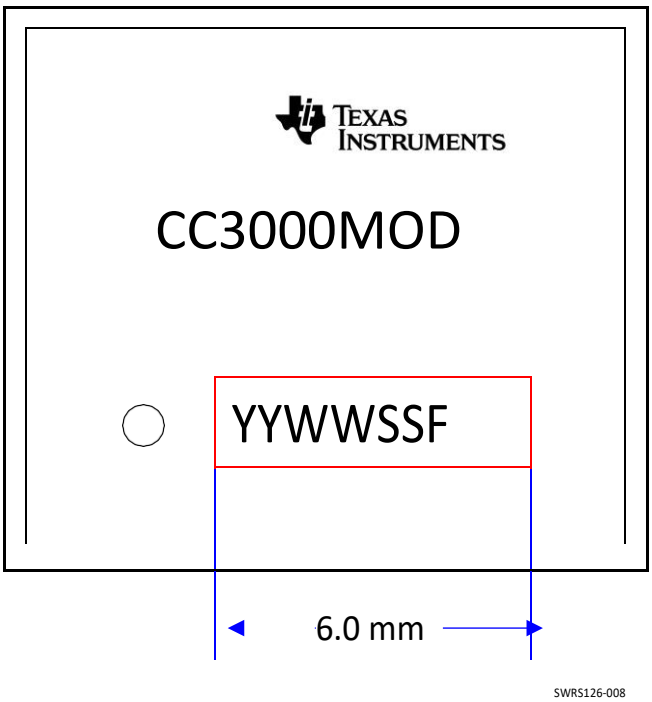


Figure 8. CC3000 Module Package Marking

Table 7. Package Marking Definitions

Code	Definition
YYWWSSF	Date
YY	Year (for example, 2012 = 12)
WW	Week (01 through 53)
SS	Serial number from 01 to 99 to match manufacturer lot number
F	Reserved for internal use

Ordering Information

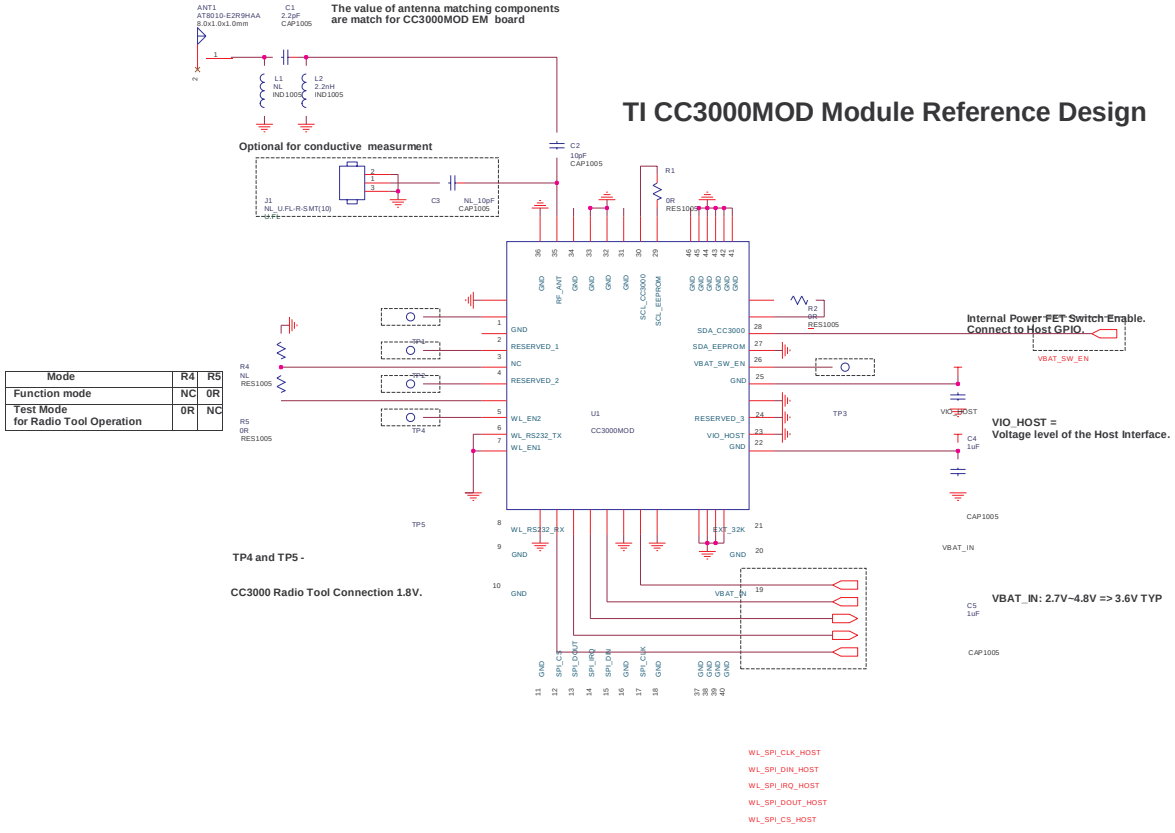
Table 8 lists the CC3000 module part numbers.

Table 8. CC3000 Module Part Numbers

Order Number	Description
CC3000MOD	CC3000 module, 44 modules per tray
CC3000MODR	CC3000 module reel, 1200 modules per reel

REFERENCE SCHEMATICS AND BILL OF MATERIALS

Figure 9 shows the schematics for the CC3000 to host reference design.



NOTE

For flexibility, VIO_HOST supports both cases in which the VBAT and VIO voltages of the MCU can be the same or different.

Table 9 lists the bill of materials.

Table 9. Bill of Materials

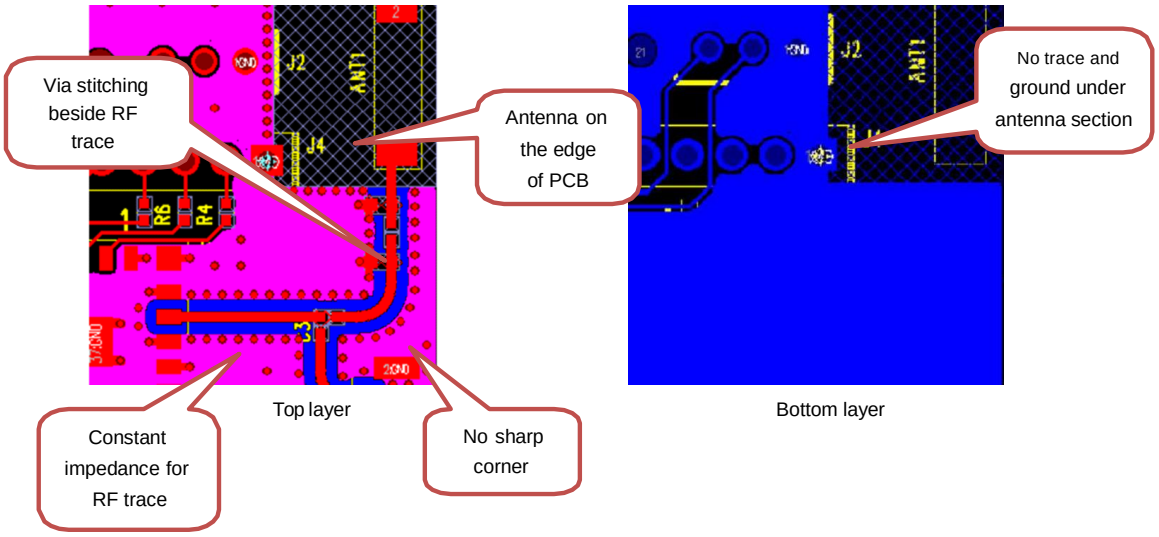
Part Reference	Description	Manufacturer	Manufacturer PN
ANT1	2.4-GHz chip antenna, 8.0 × 1.0 mm	ACX	AT8010-E2R9HAA
C1	C0402, 2.2 pF	Walsin	0402N2R2C500LT
L2	L0402, 2.2 nH	ACX	HI1005-1C2N2SMT
C2(1)	C0402, 10 pF	Walsin	0402N100J500LT
C4, C5(1)	C0402, 1 µF	Murata	GRM155R60J105KE19D
R1, R2, R5(1)	R0402, 0R	Walsin	WR04X000PTL
J1	RF coaxial U.FL, SMD	Hirose	U.FL-R-SMT-1(10)

DESIGN RECOMMENDATIONS

This section describes the layout recommendations for the CC3000 module, RF trace, and antenna.

Antenna

The ACX ceramic antenna is mounted on the CC3000 EVM board with a specific layout and matching circuit for the radiation test conducted in FCC, CE and IC certifications. Figure 10 shows the location of the antenna on the EVM board as well as the RF trace routing from the CC3000 module.



Rule Layout Recommendations

Observe the following module layout recommendations (see also Figure 11):

- Have a solid ground plane and ground vias under the module for stable system and thermal dissipation.
- Do not run signal traces underneath the module on a layer where the module is mounted.
- Signal traces can be run on a third layer under the solid ground layer and beneath the module mounting layer.

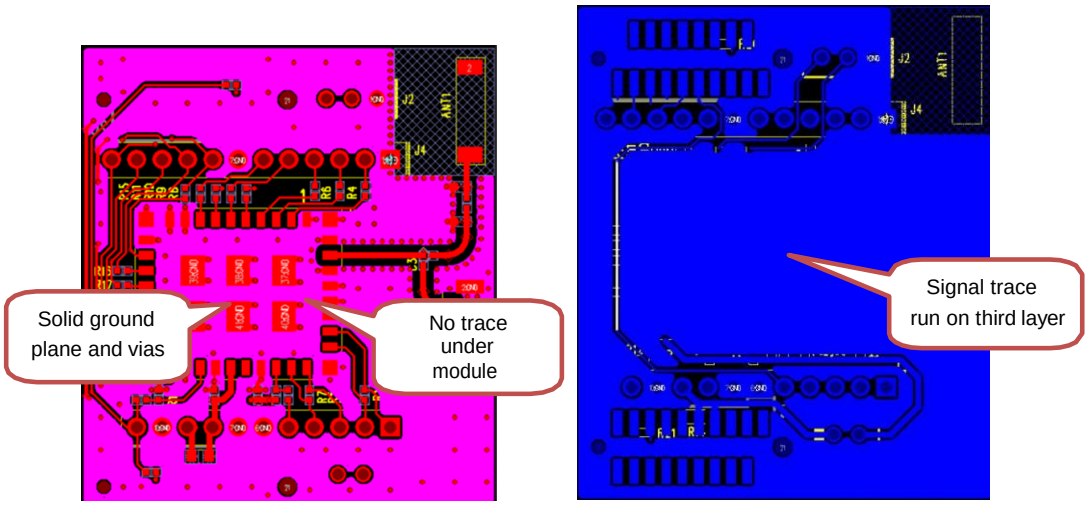


Figure 11. Module Layout

RF Trace and Antenna Layout Recommendations

Observe the following recommendations for RF trace and antenna layout (see also Figure 10):

- RF traces must have 50-Ω impedance (microstrip transmission line).
- RF trace bends must be gradual with a maximum bend of approximately 45 degrees and with trace mitered. RF traces must not have sharp corners.
- There must be no traces or ground under the antenna section.
- RF traces must have via stitching on the ground plane beside the RF trace on both sides.
- RF traces must be as short as possible. The antenna, RF traces, and the module must be on the edge of the PCB product in consideration of the product enclosure material and proximity.

ANEXO D: DATASHEET MODULO LECTOR RFID RC522.

1. Introduction

This document describes the functionality and electrical specifications of the contactless reader/writer MFRC522.

Remark: The MFRC522 supports all variants of the MIFARE Mini, MIFARE 1K, MIFARE 4K, MIFARE Ultralight, MIFARE DESFire EV1 and MIFARE Plus RF identification protocols. To aid readability throughout this data sheet, the MIFARE Mini, MIFARE 1K, MIFARE 4K, MIFARE Ultralight, MIFARE DESFire EV1 and MIFARE Plus
products and protocols have the generic name MIFARE.

1.1 Differences between version 1.0 and 2.0

The MFRC522 is available in two versions:

- MFRC52201HN1, hereafter referred to version 1.0 and
- MFRC52202HN1, hereafter referred to version 2.0.

The MFRC522 version 2.0 is fully compatible to version 1.0 and offers in addition the following features and improvements:

- Increased stability of the reader IC in rough conditions
- An additional timer prescaler, see Section 8.5.
- A corrected CRC handling when RX Multiple is set to 1

This data sheet version covers both versions of the MFRC522 and describes the differences between the versions if applicable.

2. General description

The MFRC522 is a highly integrated reader/writer IC for contactless communication at 13.56 MHz. The MFRC522 reader supports ISO/IEC 14443 A/MIFARE and NTAG.

The MFRC522's internal transmitter is able to drive a reader/writer antenna designed to communicate with ISO/IEC 14443 A/MIFARE cards and transponders without additional active circuitry. The receiver module provides a robust and efficient implementation for demodulating and decoding signals from ISO/IEC 14443 A/MIFARE compatible cards and transponders. The digital module manages the complete ISO/IEC 14443 A framing and error detection (parity and CRC) functionality.

The MFRC522 supports MF1xxS20, MF1xxS70 and MF1xxS50 products. The MFRC522 supports contactless communication and uses MIFARE higher transfer speeds up to
848 kBd in both directions.

The following host interfaces are provided:

- Serial Peripheral Interface (SPI)
- Serial UART (similar to RS232 with voltage levels dependant on pin voltage supply)
- I^2C-bus interface

3. Features and benefits

- Highly integrated analog circuitry to demodulate and decode responses
- Buffered output drivers for connecting an antenna with the minimum number of external components
- Supports ISO/IEC 14443 A/MIFARE and NTAG
- Typical operating distance in Read/Write mode up to 50 mm depending on the antenna size and tuning
- Supports MF1xxS20, MF1xxS70 and MF1xxS50 encryption in Read/Write mode
- Supports ISO/IEC 14443 A higher transfer speed communication up to 848 kBd
- Supports MFIN/MFOUT
- Additional internal power supply to the smart card IC connected via MFIN/MFOUT
- Supported host interfaces
  - SPI up to 10 Mbit/s
  - I^2C-bus interface up to 400 kBd in Fast mode, up to 3400 kBd in High-speed mode
  - RS232 Serial UART up to 1228.8 kBd, with voltage levels dependant on pin voltage supply
- FIFO buffer handles 64 byte send and receive
- Flexible interrupt modes
- Hard reset with low power function
- Power-down by software mode
- Programmable timer
- Internal oscillator for connection to 27.12 MHz quartz crystal
- 2.5 V to 3.3 V power supply
- CRC coprocessor
- Programmable I/O pins
- Internal self-test

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	analog supply voltage	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0V$	[1][2]	2.5	3.3	3.6	V
V_{DDD}	digital supply voltage			2.5	3.3	3.6	V
$V_{DD(TVDD)}$	TVDD supply voltage			2.5	3.3	3.6	V
$V_{DD(PVDD)}$	PVDD supply voltage		[3]	1.6	1.8	3.6	V
$V_{DD(SVDD)}$	SVDD supply voltage	$V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V		1.6	-	3.6	V

Table 1. Quick reference data *...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{pd}	power-down current	$V_{DDA} = V_{DDD} = V_{DD(TVDD)} = V_{DD(PVDD)}$ =3V					
		hard power-down; pin NRSTPD set LOW	[4]	-	-	5	µA
		soft power-down; RF level detector on	[4]	-	-	10	µA
I_{DDD}	digital supply current	pin DVDD; V_{DDD} =3V		-	6.5	9	mA
I_{DDA}	analog supply current	pin AVDD; V_{DDA} = 3 V, CommandReg register's RcvOff bit = 0		-	7	10	mA
		pin AVDD; receiver switched off; V_{DDA} =3 V, CommandReg register's RcvOff bit = 1		-	3	5	mA
$I_{DD(PVDD)}$	PVDD supply current	pin PVDD	[5]	-	-	40	mA
$I_{DD(TVDD)}$	TVDD supply current	pin TVDD; continuous wave	[6][7][8]	-	60	100	mA
T_{amb}	ambient temperature	HVQFN32		−25	-	+85	°C

[1] Supply voltages below 3 V reduce the performance in, for example, the achievable operating distance. [2] V_{DDA}, V_{DDD} and $V_{DD(TVDD)}$ must always be the same voltage.

[3] $V_{DD(PVDD)}$ must always be the same or lower voltage than V_{DDD}.

[4] I_{pd} is the total current for all supplies.

[5] $I_{DD(PVDD)}$ depends on the overall load at the digital pins.

[6] $I_{DD(TVDD)}$ depends on $V_{DD(TVDD)}$ and the external circuit connected to pins TX1 and TX2. [7] During typical circuit operation, the overall current is below 100 mA.

[8] Typical value using a complementary driver configuration and an antenna matched to 40 Ω between pins TX1 and TX2 at 13.56 MHz.

1. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
MFRC52201HN1/TRAYB[1]	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm	SOT617-1
MFRC52201HN1/TRAYBM[2]	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm	SOT617-1
MFRC52202HN1/TRAYB[1]	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm	SOT617-1
MFRC52202HN1/TRAYBM[2]	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm	SOT617-1

[1] Delivered in one tray. [2] Delivered in five trays.

1. Block diagram

The analog interface handles the modulation and demodulation of the analog signals.

The contactless UART manages the protocol requirements for the communication protocols in cooperation with the host. The FIFO buffer ensures fast and convenient data transfer to and from the host and the contactless UART and vice versa.

Various host interfaces are implemented to meet different customer requirements.

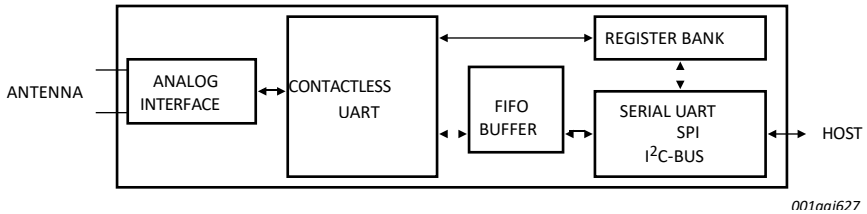


Fig 1. Simplified block diagram of the MFRC522

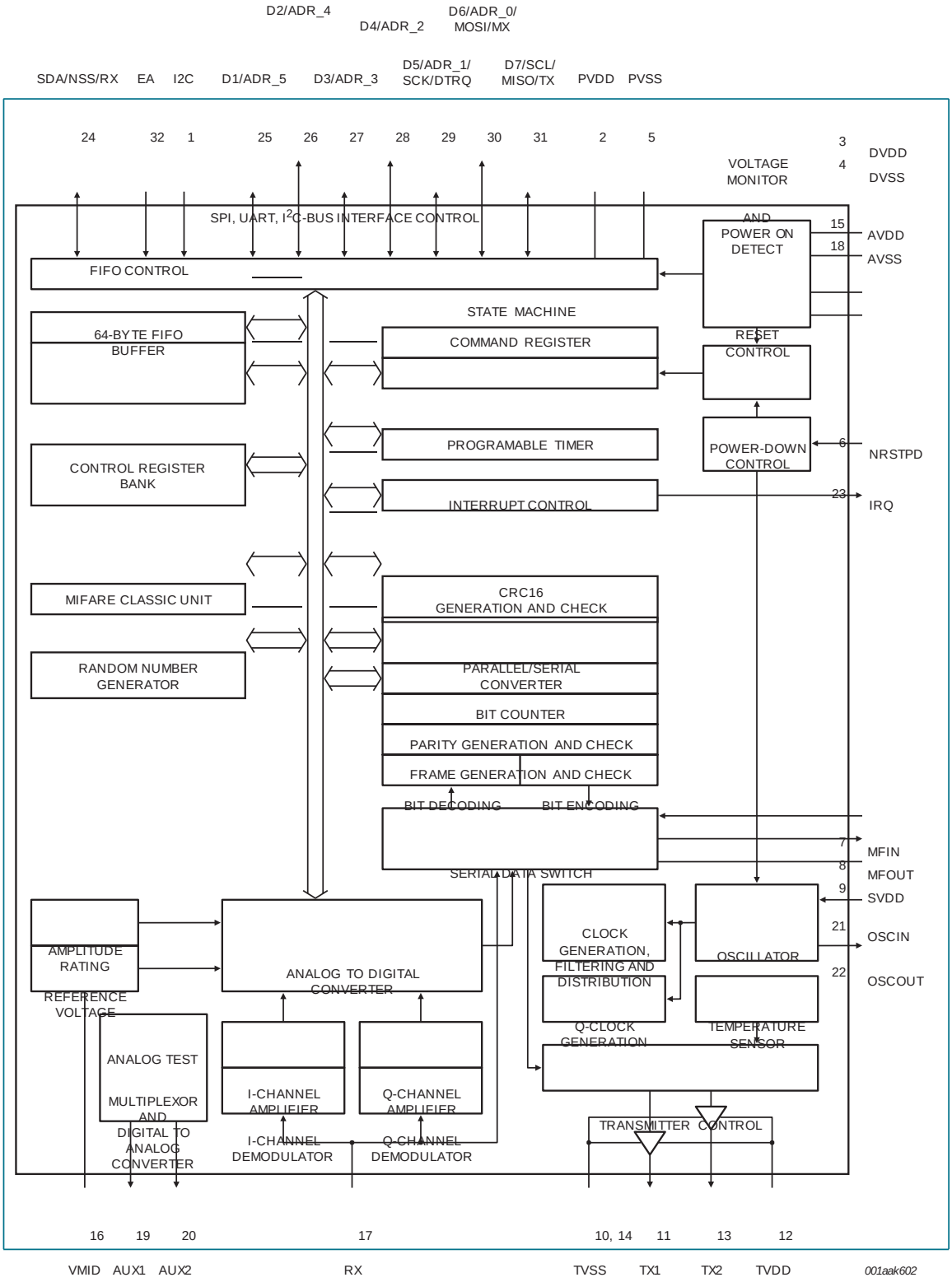


Fig 2. Detailed block diagram of the MFRC522

1. Pinning information

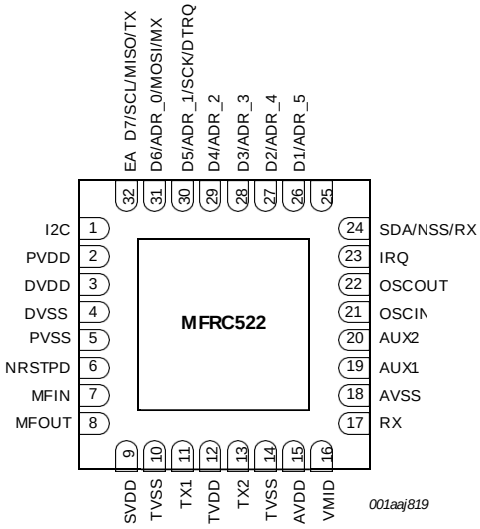


Fig 3. Pinning configuration HVQFN32 (SOT617-1)

1.1 Pin description

Table 3. Pin description

Pin	Symbol	Type[1]	Description
1	I2C	I	I^2C-bus enable input[2]
2	PVDD	P	pin power supply
3	DVDD	P	digital power supply
4	DVSS	G	digital ground[3]
5	PVSS	G	pin power supply ground
6	NRSTPD	I	reset and power-down input: power-down: enabled when LOW; internal current sinks are switched off, the oscillator is inhibited and the input pins are disconnected from the outside world reset: enabled by a positive edge
7	MFIN	I	MIFARE signal input
8	MFOUT	O	MIFARE signal output
9	SVDD	P	MFIN and MFOUT pin power supply
10	TVSS	G	transmitter output stage 1 ground
11	TX1	O	transmitter 1 modulated 13.56 MHz energy carrier output
12	TVDD	P	transmitter power supply: supplies the output stage of transmitters 1 and 2
13	TX2	O	transmitter 2 modulated 13.56 MHz energy carrier output
14	TVSS	G	transmitter output stage 2 ground
15	AVDD	P	analog power supply

Table 3. Pin description *...continued*

Pin	Symbol	Type[1]	Description
16	VMID	P	internal reference voltage
17	RX	I	RF signal input
18	AVSS	G	analog ground
19	AUX1	O	auxiliary outputs for test purposes
20	AUX2	O	auxiliary outputs for test purposes
21	OSCIN	I	crystal oscillator inverting amplifier input; also the input for an externally generated clock (f_{clk} = 27.12 MHz)
22	OSCOUT	O	crystal oscillator inverting amplifier output
23	IRQ	O	interrupt request output: indicates an interrupt event
24	SDA	I/O	I^2C-bus serial data line input/output[2]
	NSS	I	SPI signal input[2]
	RX	I	UART address input[2]
25	D1	I/O	test port[2]
	ADR_5	I/O	I^2C-bus address 5 input[2]
26	D2	I/O	test port
	ADR_4	I	I^2C-bus address 4 input[2]
27	D3	I/O	test port
	ADR_3	I	I^2C-bus address 3 input[2]
28	D4	I/O	test port
	ADR_2	I	I^2C-bus address 2 input[2]
29	D5	I/O	test port
	ADR_1	I	I^2C-bus address 1 input[2]
	SCK	I	SPI serial clock input[2]
	DTRQ	O	UART request to send output to microcontroller[2]
30	D6	I/O	test port
	ADR_0	I	I^2C-bus address 0 input[2]
	MOSI	I/O	SPI master out, slave in[2]
	MX	O	UART output to microcontroller[2]
31	D7	I/O	test port
	SCL	I/O	I^2C-bus clock input/output[2]
	MISO	I/O	SPI master in, slave out[2]
	TX	O	UART data output to microcontroller[2]
32	EA	I	external address input for coding I^2C-bus address[2]

[1] Pin types: I = Input, O = Output, I/O = Input/Output, P = Power and G = Ground. [2] The pin functionality of these pins is explained in Section 8.1 “Digital interfaces”.

[3] Connection of heatsink pad on package bottom side is not necessary. Optional connection to pin DVSS is posible.

1. Functional description

The MFRC522 transmission module supports the Read/Write mode for ISO/IEC 14443 A/MIFARE using various transfer speeds and modulation protocols.

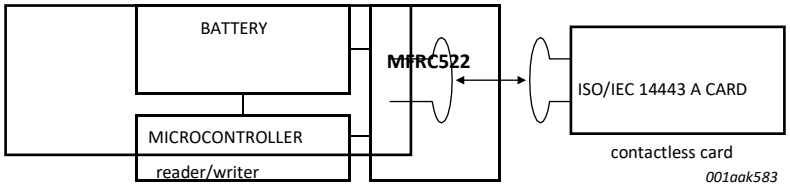
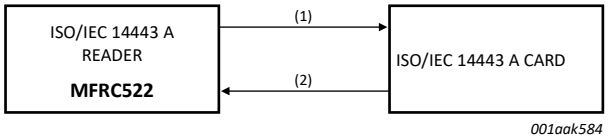


Fig 4. MFRC522 Read/Write mode

The physical level communication is shown in Figure 5.



(1) Reader to card 100 % ASK, Miller encoded, transfer speed 106 kBd to 848 kBd.

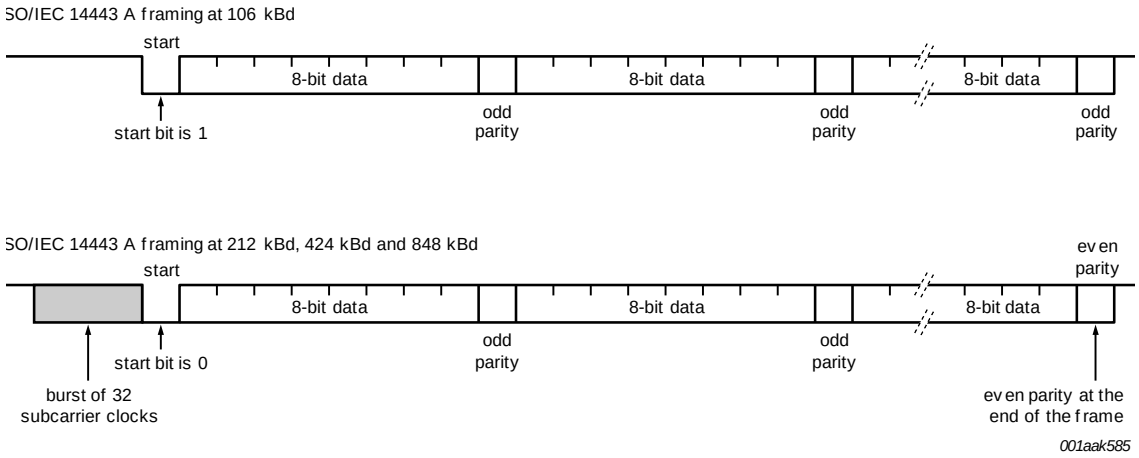
(2) Card to reader subcarrier load modulation, Manchester encoded or BPSK, transfer speed 106 kBd to 848 kBd.

The physical parameters are described in Table 4.

Table 4. Communication overview for ISO/IEC 14443 A/MIFARE reader/writer

Communication direction	Signal type	Transfer speed			
		106 kBd	212 kBd	424 kBd	848 kBd
Reader to card (send data from the MFRC522 to a card)	reader side modulation	100 % ASK	100 % ASK	100 % ASK	100 % ASK
	bit encoding	modified Miller encoding	modified Miller encoding	modified Miller	modified Miller encoding
	bit length	128 (13.56 µs)	64 (13.56 µs)	32 (13.56 µs)	16 (13.56 µs)
Card to reader (MFRC522 receives data from a card)	card side modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz / 16	13.56 MHz / 16	13.56 MHz / 16	13.56 MHz / 16
	bit encoding	Manchester encoding	BPSK	BPSK	BPSK

The MFRC522's contactless UART and dedicated external host must manage the complete ISO/IEC 14443 A/MIFARE protocol. Figure 6 shows the data coding and framing according to ISO/IEC 14443 A/MIFARE.



Data coding and framing according to ISO/IEC 14443 A

The internal CRC coprocessor calculates the CRC value based on ISO/IEC 14443 A part 3 and handles parity generation internally according to the transfer speed. Automatic parity generation can be switched off using the MfRxReg register's ParityDisable bit.

1.1 Digital interfaces

8.1.1 Automatic microcontroller interface detection

The MFRC522 supports direct interfacing of hosts using SPI, I^2C-bus or serial UART interfaces. The MFRC522 resets its interface and checks the current host interface type automatically after performing a power-on or hard reset. The MFRC522 identifies the host interface by sensing the logic levels on the control pins after the reset phase. This is done using a combination of fixed pin connections. Table 5 shows the different connection configurations.

Table 5. Connection protocol for detecting different interface types

Pin	Interface type		
	UART (input)	SPI (output)	I^2C-bus (I/O)
SDA	RX	NSS	SDA
I2C	0	0	1
EA	0	1	EA
D7	TX	MISO	SCL
D6	MX	MOSI	ADR_0
D5	DTRQ	SCK	ADR_1
D4	-	-	ADR_2
D3	-	-	ADR_3
D2	-	-	ADR_4
D1	-	-	ADR_5

8.1.1 Serial Peripheral Interface

A serial peripheral interface (SPI compatible) is supported to enable high-speed communication to the host. The interface can handle data speeds up to 10 Mbit/s. When communicating with a host, the MFRC522 acts as a slave, receiving data from the external host for register settings, sending and receiving data relevant for RF interface communication.

An interface compatible with SPI enables high-speed serial communication between the MFRC522 and a microcontroller. The implemented interface is in accordance with the SPI standard.

The timing specification is given in Section 14.1 on page 78.

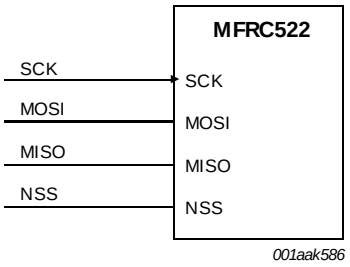


Fig 7. SPI connection to host

The MFRC522 acts as a slave during SPI communication. The SPI clock signal SCK must be generated by the master. Data communication from the master to the slave uses the MOSI line. The MISO line is used to send data from the MFRC522 to the master.

Data bytes on both MOSI and MISO lines are sent with the MSB first. Data on both MOSI and MISO lines must be stable on the rising edge of the clock and can be changed on the falling edge. Data is provided by the MFRC522 on the falling clock edge and is stable during the rising clock edge.

8.1.1.1 SPI read data

Reading data using SPI requires the byte order shown in Table 6 to be used. It is possible to read out up to n-data bytes.

The first byte sent defines both the mode and the address.

Table 6. MOSI and MISO byte order

Line	Byte 0	Byte 1	Byte 2	To	Byte n	Byte n + 1
MOSI	address 0	address 1	address 2	...	address n	00
MISO	X[1]	data 0	data 1	...	data n – 1	data n

[1] X = Do not care.

Remark: The MSB must be sent first.

8.1.1.1 SPI write data

To write data to the MFRC522 using SPI requires the byte order shown in Table 7. It is possible to write up to n data bytes by only sending one address byte.

The first send byte defines both the mode and the address byte.

Table 7. MOSI and MISO byte order

Line	Byte 0	Byte 1	Byte 2	To	Byte n	Byte n + 1
MOSI	address 0	data 0	data 1	...	data n – 1	data n
MISO	X[1]	X[1]	X[1]	...	X[1]	X[1]

[1] X = Do not care.

Remark: The MSB must be sent first.

8.1.1.2 SPI address byte

The address byte must meet the following format.

The MSB of the first byte defines the mode used. To read data from the MFRC522 the MSB is set to logic 1. To write data to the MFRC522 the MSB must be set to logic 0. Bits 6 to 1 define the address and the LSB is set to logic 0.

Table 8. Address byte 0 register; address MOSI

7 (MSB)	6	5	4	3	2	1	0 (LSB)
1 = read 0 = write	address						0

8.1.2 UART interface

8.1.2.1 Connection to a host

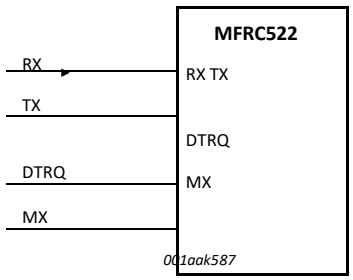


Fig 8. UART connection to microcontrollers

Remark: Signals DTRQ and MX can be disabled by clearing TestPinEnReg register's RS232LineEn bit.

8.1.1.1 *Selectable UART transfer speeds*

The internal UART interface is compatible with an RS232 serial interface.

The default transfer speed is 9.6 kBd. To change the transfer speed, the host controller must write a value for the new transfer speed to the SerialSpeedReg register. Bits BR_T0[2:0] and BR_T1[4:0] define the factors for setting the transfer speed in the SerialSpeedReg register.

The BR_T0[2:0] and BR_T1[4:0] settings are described in Table 9. Examples of different transfer speeds and the relevant register settings are given in Table 10.

Table 9. BR_T0 and BR_T1 settings

BR_Tn	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
BR_T0 factor	1	1	2	4	8	16	32	64
BR_T1 range	1 to 32	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64

Table 10. Selectable UART transferspeeds

Transfer speed (kBd)	SerialSpeedReg value		Transfer speed accuracy (%)[1]
	Decimal	Hexadecimal	
7.2	250	FAh	–0.25
9.6	235	EBh	0.32
14.4	218	DAh	–0.25
19.2	203	CBh	0.32
38.4	171	ABh	0.32
57.6	154	9Ah	–0.25
115.2	122	7Ah	–0.25
128	116	74h	–0.06
230.4	90	5Ah	–0.25
460.8	58	3Ah	–0.25
921.6	28	1Ch	1.45
1228.8	21	15h	0.32

[1] The resulting transfer speed error is less than 1.5 % for all described transfer speeds.

The selectable transfer speeds shown in Table 10 are calculated according to the following equations:

If BR_T0[2:0] = 0:

8.1.1.1 UART framing

Table 11. UART framing

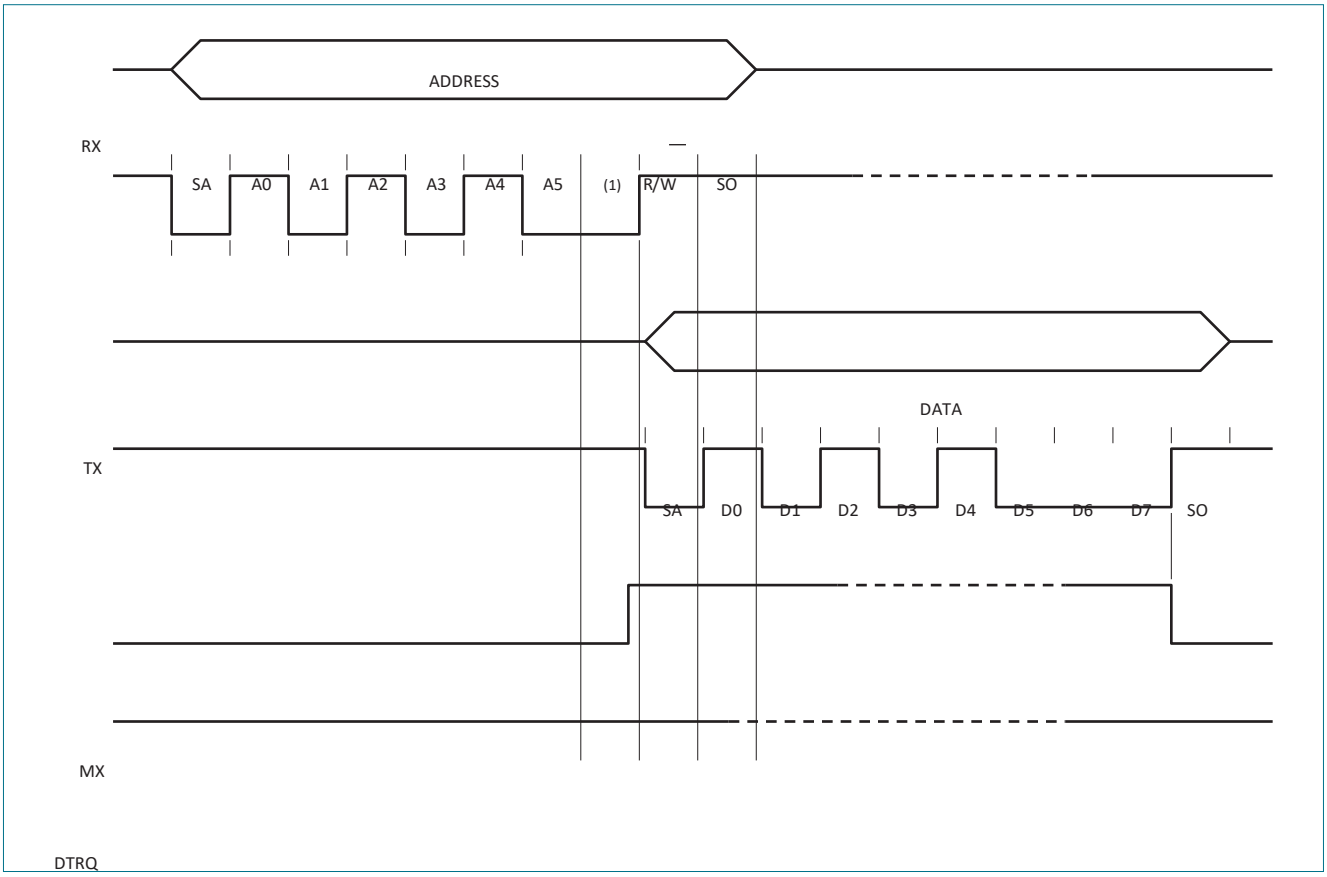
Bit	Length	Value
Start	1-bit	0
Data	8 bits	data
Stop	1-bit	1

Remark: The LSB for data and address bytes must be sent first. No parity bit is used during transmission.

Read data: To read data using the UART interface, the flow shown in Table 12 must be used. The first byte sent defines both the mode and the address.

Table 12. Read data byte order

Pin	Byte 0	Byte 1
RX (pin 24)	address	-
TX (pin 31)	-	data 0



Write data: To write data to the MFRC522 using the UART interface, the structure shown in Table 13 must be used.

The first byte sent defines both the mode and the address

8.1.1 I²C-bus interface

An I²C-bus (Inter-IC) interface is supported to enable a low-cost, low pin count serial bus interface to the host. The I²C-bus interface is implemented according to NXP Semiconductors' *I²C-bus interface specification, rev. 2.1, January 2000*. The interface can only act in Slave mode. Therefore the MFRC522 does not implement clock generation or access arbitration.

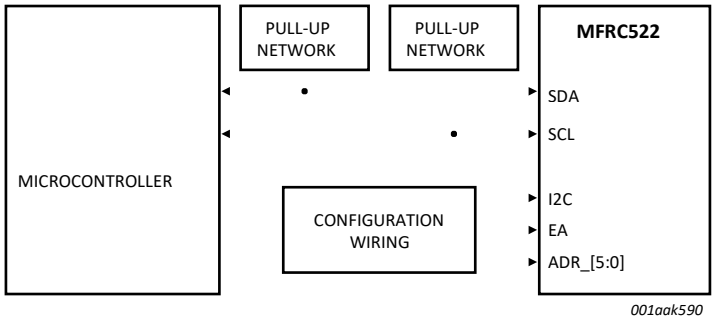


Fig 11. I²C-bus interface

The MFRC522 can act either as a slave receiver or slave transmitter in Standard mode, Fast mode and High-speed mode.

SDA is a bidirectional line connected to a positive supply voltage using a current source or a pull-up resistor. Both SDA and SCL lines are set HIGH when data is not transmitted. The MFRC522 has a 3-state output stage to perform the wired-AND function. Data on the I²C-bus can be transferred at data rates of up to 100 kBd in Standard mode, up to 400 kBd in Fast mode or up to 3.4 Mbit/s in High-speed mode.

If the I²C-bus interface is selected, spike suppression is activated on lines SCL and SDA as defined in the I²C-bus interface specification.

See Table 155 on page 79 for timing requirements.

ANEXO E: TEST DE USUARIO I PROTOTIPO

Este test de Usuario se realiza dentro de la etapa de desarrollo del sistema, como parte del Diseño Centrado en el Usuario tratado en el capítulo tres de este proyecto, se lanza entre los clientes habituales de Ecociclo, que ya habían tenido interacción con el sistema mecánico primario del sistema. Este Test de usuario se basa en algunos test de usabilidad y calidad previstos en variada bibliografía como el Libro de Evaluación de Lores y Agosat de la Universidad de Lleida y bibliografía del Congreso de Chile por Felipe Salmazan y Juan Camus .

El test consiste en una serie de preguntas que se realizan a los usuarios y de acuerdo con sus respuestas, se determinan las características a mejorar dentro del sistema. La Prueba está enfocada a los siguientes ámbitos:

• Contenido
• Navegación
• Gráfica Web
• Feedback
• Utilidad

Esta división se hace con el fin de establecer y evaluar los aspectos de usabilidad, aplicación y respuesta de la plataforma del SBC.

- *Preguntas sobre Identidad:* En este ámbito se busca establecer si el sitio logra diferenciarse de otros, por ello, las preguntas se enfocan especialmente a determinar si a primera vista el usuario ha entendido en qué espacio ha ingresado. Lo que se busca es obtener la “primera impresión” del usuario. Una vez que se ha terminado este grupo de preguntas, se debe invitar al usuario a navegar en el sitio, con el objetivo de responder los siguientes interrogantes de la prueba.

-*Preguntas sobre Contenido*: Las preguntas de esta sección y de las siguientes, se realizan durante la navegación del usuario en la plataforma, con el fin de que se forme una opinión acerca de lo que está viendo y la forma de navegar por sus contenidos. Su objetivo es determinar la calidad que le asigna a los contenidos y si la forma de presentarlos le permite hacerse una idea concreta de la información que se le está entregando través del sitio web.

-*Preguntas sobre Navegación*: Las preguntas de esta sección permiten establecer si la forma de organizar la información dentro del sitio web es adecuada de acuerdo con la experiencia, conocimientos y expectativas que tenga el usuario que visite el sitio web.

-*Preguntas sobre Gráfica Web*: Las preguntas de esta sección buscan establecer si al usuario le ayuda la información gráfica del sitio web, como también su percepción acerca de la velocidad de despliegue de cada interfaz.

-*Preguntas sobre Feedback:* Las preguntas de esta sección buscan establecer si las respuestas de la plataforma hacia las órdenes del usuario son claras, rápidas y eficientes.

-*Preguntas sobre Utilidad*: Las preguntas de esta sección son las finales de la prueba y tienen el objetivo de establecer una especie de resumen general de la experiencia de navegar el sitio.

Test de usuario:

En las figuras 1-4 se presenta el Test de Usuario formulado y analizado.

TEST DE USAURIO

Nombre _____

Profesión: _____

Tiene experiencia en
Internet?_____

_____

¿Navega habitualmente? ¿Cuánto tiempo dedica a ello en el día? _____

_____

¿Conoce algún sistema de Bicicleta Publicas en alguna otra ciudad? _____

_____

Sección de Preguntas: Antes de comenzar con las preguntas sobre el sitio, a medida que desarrolle las acciones sobre este, vaya manifestando en voz alta sus impresiones acerca de cada interfaz de la plataforma.

Identidad:

- ¿De los elementos que se muestran en la pantalla, hay algo que crea esta fuera de lugar o no representa al sitio? _____

_____

-Las gráficas son correspondiente al servicio que presta la plataforma? _____

_____

_____

-Es claro los elementos de contacto de la administración del Sitio? ¿Le fue fácil encontrarlos? ____

_____

Contenido:

-Es adecuada la selección de los contenidos destacados en cada interfaz de la plataforma? _____

_____

_____

Figura 1. Test de Usuario Planilla 1

-En la portada de inicio son claras las secciones en las cuales se subdivide el proceso de préstamo de las bicicletas? ¿Por qué? _____

_____

_____

-En la portada de inicio está expuesta adecuadamente toda la información del servicio que se presta?_____

_____

_____

-Los textos usados y los recuadros de los mensajes de indicaciones son suficientes y pertinentes? _

_____

_____

Navegación:

-Es claro el proceso de navegación por el sitio? _____

_____

_____

-Los encabezados y los elementos de ayuda y de flujo (atrás y adelante) son claros?

_____

_____

-La información que le ofrece la plataforma es suficiente para ubicarse en que parte del proceso del servicio está usted en cualquier momento? _____

_____

_____

-La respuesta del sitio es rápida y eficiente? ¿Es completamente entendible? _____

_____

_____

Grafica Web

-Las secciones gráficas para realizar el préstamo de la bicicleta son claras? ¿Ha logrado distinguir el juego de los colores en las estaciones gráficas para mostrar la disponibilidad de las bicicletas? _____

_____

_____

-Le pareció adecuada las forma en las que se muestran las imágenes ene l sitio web? _____

_____

_____

-Las imágenes cargan correctamente ¿Cree que la velocidad del sitio es buena? _____

Figura 2.Test de Usuario Planilla 2

_____

_____

-Qué gráfica le ha llamado más la atención? ¿Como la mejoraría? _____

_____

-Considera que gráficamente el sitio esta equilibrado, muy simple o recargado? _____

_____

_____

Feedback

- ¿Al enviar datos mediante el sitio, la plataforma le avisa si los ha recibido correctamente o no? __

_____

_____

-La respuesta a las indicaciones hacia el SBC son eficientes? _____

_____

-La respuesta del servicio de préstamo es buena_____

_____

-Qué mejoraría en el proceso de préstamo de las bicicletas? _____

_____

_____

Utilidad

-Tras esta primera navegación, ¿Son claros los procesos que se realizan a través de la plataforma para obtener o entregar una bici? _____

_____

_____

-Cree que los contenidos y el servicio de préstamo que ofrece la plataforma son útiles realmente?

_____

_____

-Qué es lo que más le llamo la atencion positivamente o negativamente del sitio web en general?

_____

_____

-Respecto al sistema mecánico de préstamo que se tenia antes. ¿Cree que la plataforma lo mejora o empora y porqué?

Figura 3.Test de Usuario Planilla 3.

La ficha técnica del estudio realizado se presenta en la tabla 1.

FICHA TECNICA
Técnica de Recolección de Datos: Cuestionario Físico
Grupo Objetivo: Usuarios activos en el Sistema Ecociclo
Universo: 342 usuarios activados (Fecha de corte Marzo 2016)
Tamaño de Muestra: 90 (usuarios más antiguos y frecuentes)
Temas Consultados: Integración de la Plataforma al SBC de Ecociclo
Fecha de realización del estudio: Enero de 2016 a Febrero de 2016
Margen de Error: 4,2%
Fecha de Prueba Piloto: enero 2016
Fecha de Prueba Piloto 2: Marzo de 2016
Variables: Categóricas y Numéricas
Clasificación: Encuesta de opinión parcial directa con preguntas abiertas

Tabla 1. Ficha Técnica Test de Usuario Ecociclo.

-Resultados:

Posterior a la recolección de los test realizados se analizó cada una de las respuestas entregadas por los usuarios del sistema, se determinó que la integración de la plataforma al SBC inicial con el que ya estaban familiarizados fue según la figura 4 buena, aunque con variadas recomendaciones en cuanto a la navegación, el flujo de los procesos y las gráficas de la misma. A continuación, se en listan las sugerencias más recurrentes:

-Mejorar las gráficas de cada interfaz de la plataforma, en especial la secciónе inicio y el proceso de préstamo.

-Aumentar la cantidad de mensajes con indicaciones acerca de los pasos de cada proceso para aumentar su claridad ante el usuario.

-Aumentar los vectores en cada interfaz para mejorar la apariencia general del sitio.

-Mejorar la información del proceso de préstamo colocando un paso a paso antes de iniciar este dicho proceso.

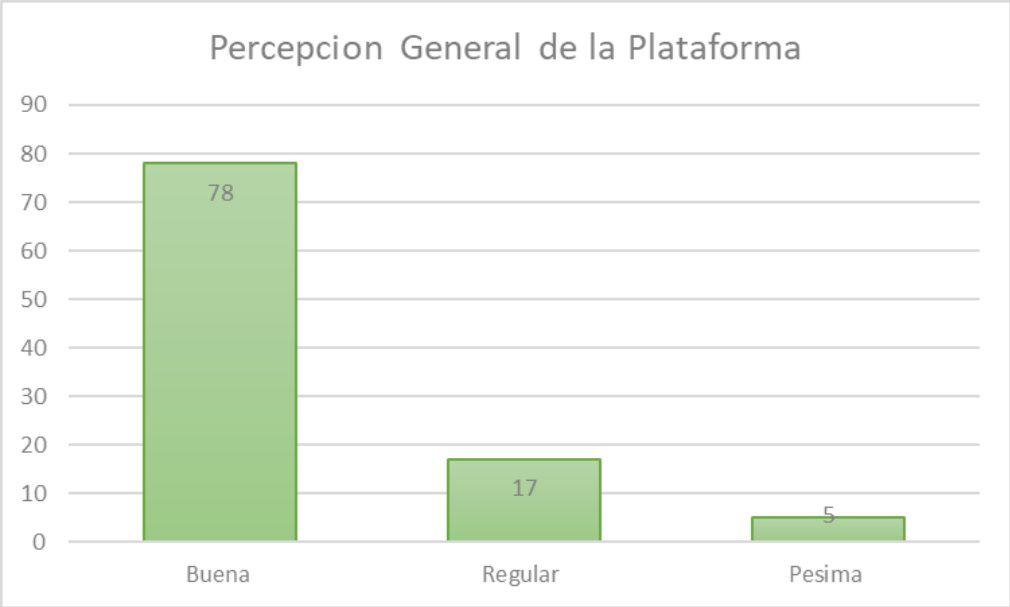


Figura 4.Percpcion General de la Plataforma Web de Ecociclo.

ANEXO F: FORMULARIO DE SERVICIO ECOCICLO:

En la Figura 5 y 6 se presenta el Formulario de Servicio de Ecociclo que se presentó a los clientes después del lanzamiento oficial de la nueva estación de préstamos.

ecociclo.co

Bicicletas Públicas

Formulario Ecociclo-Arcossoft

Nombre y apellidos: _____

Edad: _____ Sexo: _____ Nacionalidad _____

Fecha: _____ Ocupación: _____

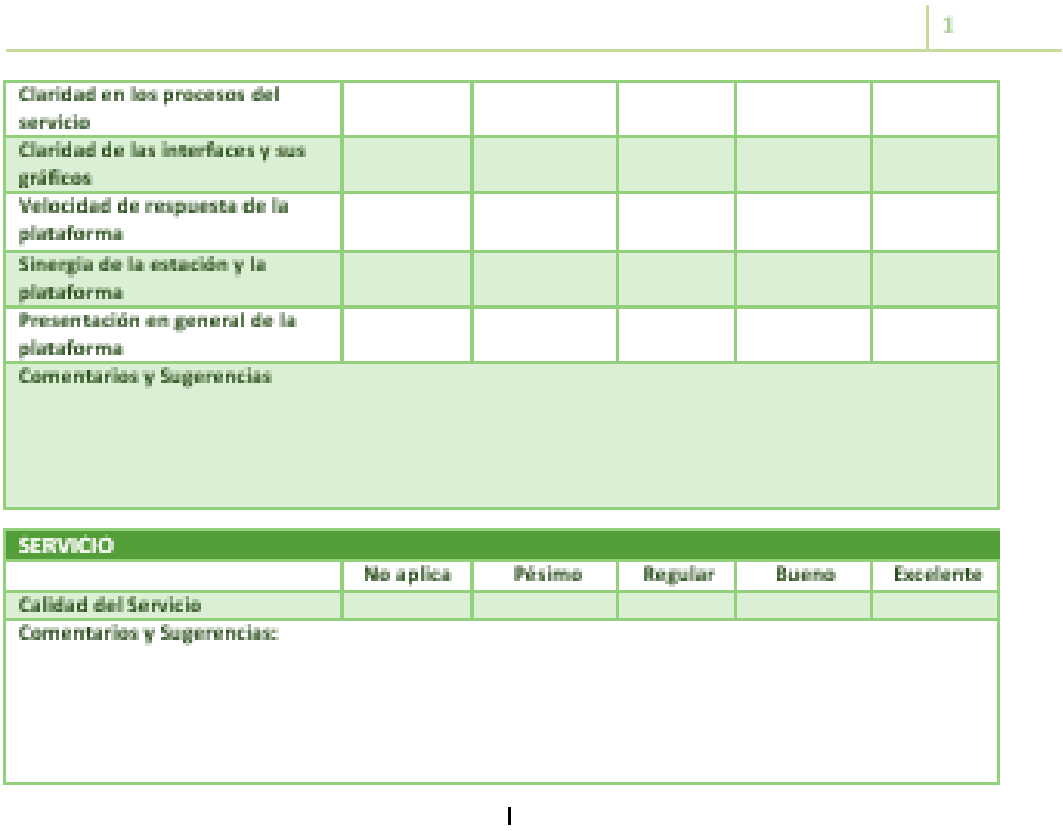
Marque con una X la puntuación que considere más acorde con el servicio recibido.

BICICLETA	No aplica	Pésimo	Regular	Bueno	Excelente
Comodidad de la bicicleta					
Funcionalidad de la bicicleta					
Confiabilidad de la bicicleta					
Disponibilidad de la bicicleta					
Comentarios y Sugerencias:					

ESTACION AUTOMATICA	No aplica	Pésimo	Regular	Bueno	Excelente
Funcionalidad de las estaciones					
Facilidad para entregar una bici					
Facilidad para retirar una bici					
Sistema de aviso de retiro					
Control de servicio					
Comentarios y Sugerencias					

PLATAFORMA	No aplica	Pésimo	Regular	Bueno	Excelente
Facilidad de interacción					

Figura 5.Formulario de Servicio Ecociclo Planilla 1.



Claridad en los procesos del servicio					
Claridad de las interfaces y sus gráficos					
Velocidad de respuesta de la plataforma					
Sinergia de la estación y la plataforma					
Presentación en general de la plataforma					
Comentarios y Sugerencias					

SERVICIO					
	No aplica	Pésimo	Regular	Bueno	Excelente
Calidad del Servicio					
Comentarios y Sugerencias:					

Figura 6.Formulario de Servicio Ecociclo Planilla 2.

Objetivo: Conocer la percepción que tienen los usuarios Ecociclo sobre el servicio que ofrece el Sistema de Bicicletas y conocer el nivel de satisfacción acerca de los despachadores, las bicicletas, disponibilidad de la flota y estado de las estaciones. Además, conocer cuáles son sus recomendaciones y sugerencias para mejorar el sistema. La ficha técnica del estudio realizado se presenta en la Tabla 2.

FICHA TECNICA
Técnica de Recolección de Datos: Cuestionario Físico
Grupo Objetivo: Usuarios activos en el Sistema Ecociclo
Universo: 450 usuarios activados (Fecha de corte Julio 2016)
Tamaño de Muestra: 200
Temas Consultados: Percepción del sistema y nivel de satisfacción
Fecha de realización del estudio: Mayo de 2016 a Junio de 2016
Margen de Error: 4,5%
Fecha de Prueba Piloto: Enero 2016
Fecha de Prueba Piloto 2: Mayo de 2016
Variables: Categóricas y Numéricas
Clasificación: Encuesta de opinión parcial directa con preguntas cerradas y abiertas

Tabla 2.Ficha Técnica Formulario de Servicio de Ecociclo.

-Resultado de las encuestas desagregado cualitativamente:

1.El público que utiliza el Sistema de Bicicletas Ecociclo es joven, con el 71% de edades desde los 18 a los 35 años. (Ver tabla 3 y Figura 7) .

EDAD	
RANGO	**CUENTA DE EDAD**
18-25	96
26-35	46
36-45	26
46-55	17
56-65	13
66-75	2
TOTAL	**200**

Tabla 3.Rango de Edades de los Usuarios Ecociclo.

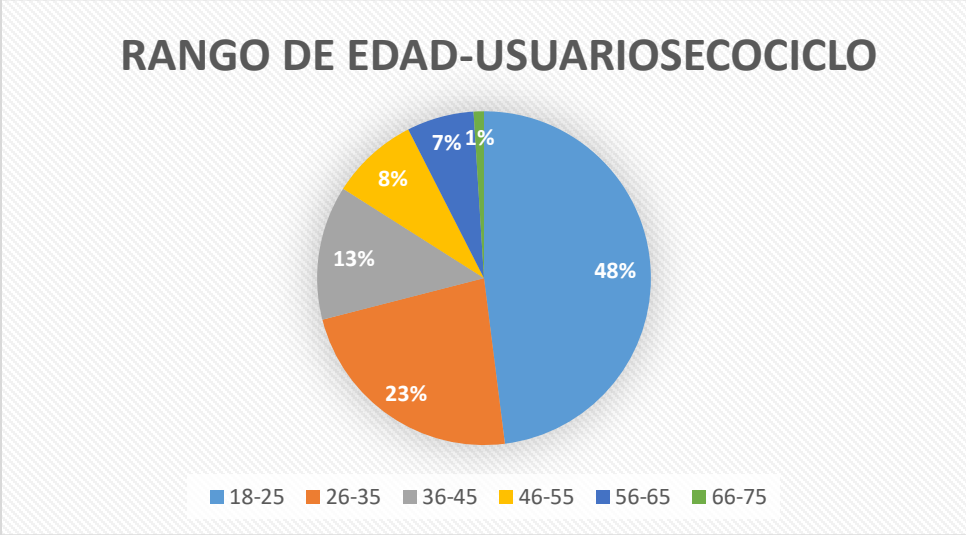


Figura 7.Grafico Rango de Edades de Usuarios Ecociclo.

El principal usuario de Ecociclo es el estudiante universitario con un 51% seguido de los trabajadores o empleados con un 27% de participación. (Ver tabla 4 y Figura 8)

OCUPACION	
ETIQUETA	**CUENTA**
DESEMPLEADO	17
ESTUDIANTE	102
TRABAJADOR/EMPLEADO	53
JUBILADO	6
OTRO , CUAL?	22

TOTAL	200

Tabla 4.Tipo de Ocupación de los Usuarios de Ecociclo.

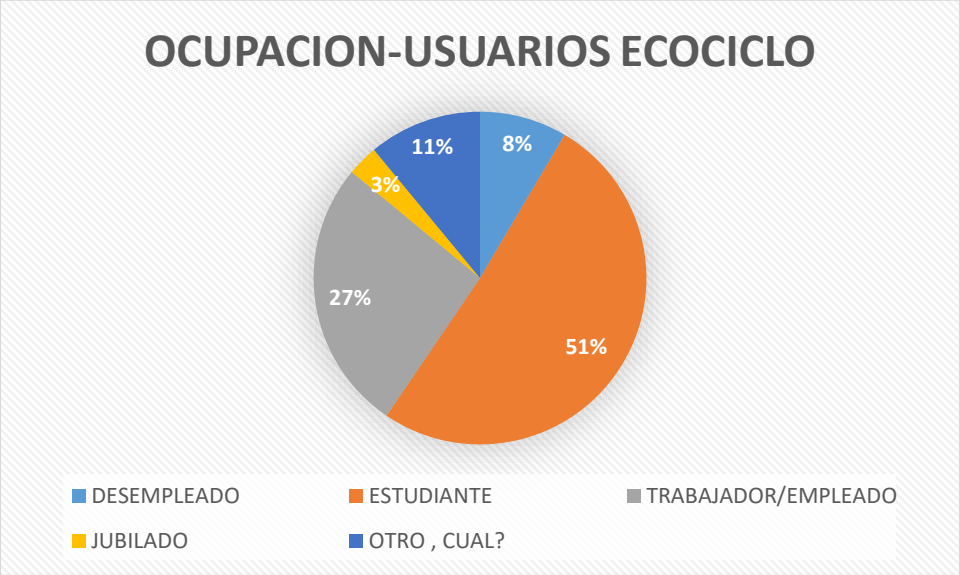


Figura 8. Gráfico de tipo de Ocupación de los Usuarios de Ecociclo.

Los usuarios de Ecociclo son en su mayoría hombres con un 68% mientras las muejres representan un 32% de participación. (Ver tabla 4 y Figura 8)

SEXO	
ETIQUETA	**CUENTA**
MASCULINO	136
FEMENINO	64
TOTAL	**200**

Tabla 5. Sexo de los Usuarios de Ecociclo.

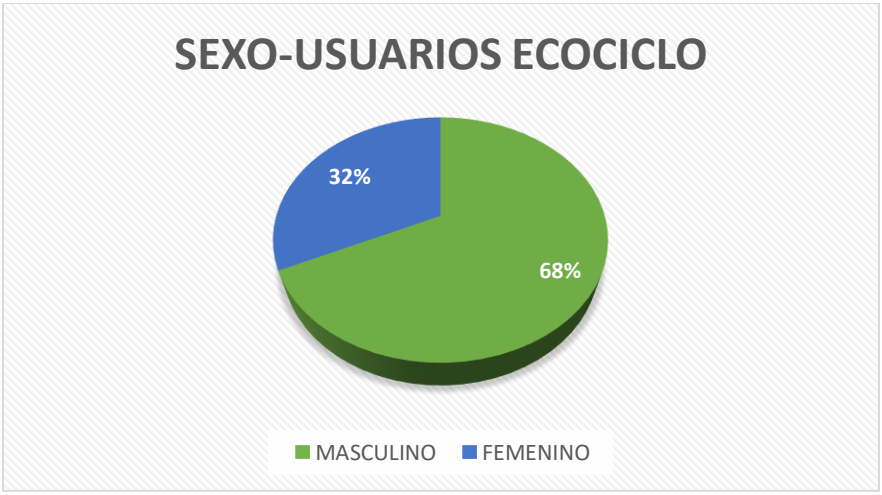


Figura 9. Sexo de los Usuarios de Ecociclo.

Para este proyecto se tomarán los resultados obtenidos para la Estación Automática, la Plataforma y el Servicio.

-Estación Automática:

En la Tabla 6 se presentan los resultados obtenidos para la Estación Automática del Sistema de Ecociclo.

ESTACION AUTOMATICA						
	No aplica	**Pésimo**	**Regular**	**Bueno**	**Excelente**	**TOTAL**
Funcionalidad de las estaciones	2	0	10	34	154	200
Facilidad para entregar una bici	0	0	2	187	11	200
Facilidad para retirar una bici	0	0	1	72	127	200
Sistema de aviso de retiro	0	0	12	56	132	200
Control de servicio	2	0	9	123	66	200

Tabla 6. Resultados obtenidos acerca de la Estación Automática.

- La funcionalidad general de las estaciones es del 94% entre excelente y bueno. (Ver Figura 10)

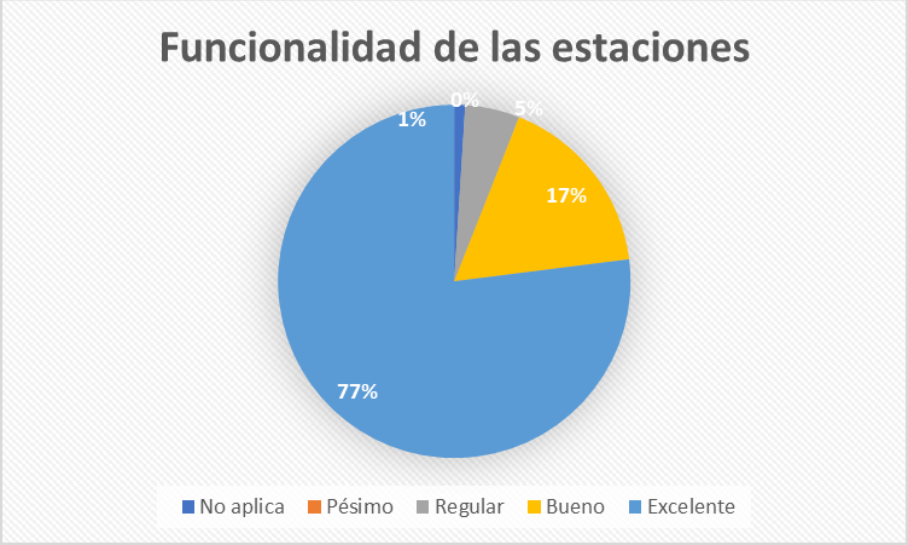


Figura 10. Grafica de la Funcionalidad de las Estaciones Automáticas.

- La facilidad para entregar bicicletas en la estación es del 99% entre excelente y bueno. (Ver Figura 11)

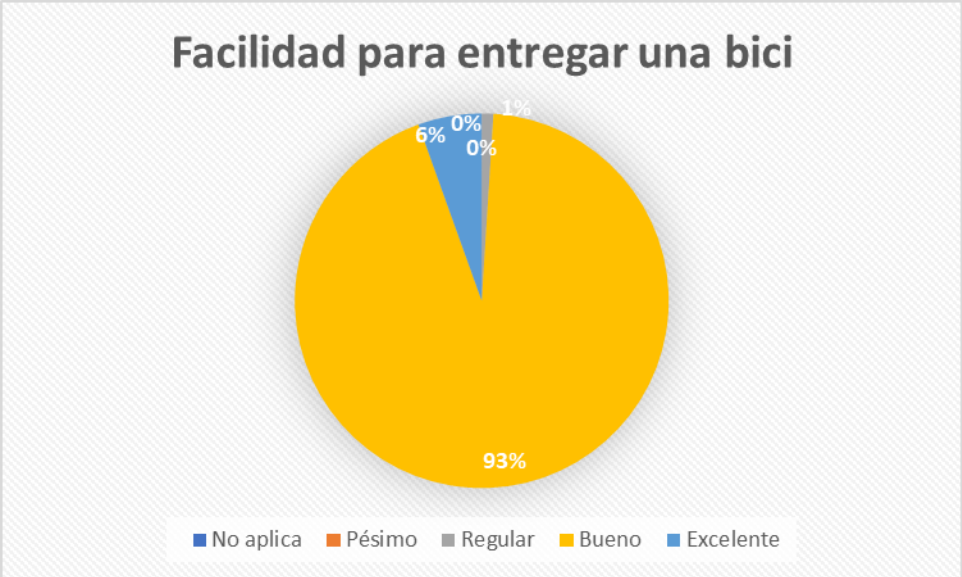


Figura 11.Grafica Facilidad para Entregar las Bicicletas.

- La facilidad para retirar las bicicletas en la estación es del 99% entre excelente y bueno. (Ver Figura 12)

Figura 12.Grafica Facilidad para Retirar las Bicicletas.

- El sistema de aviso de retiro de la bicicleta en la estación es del 94% entre excelente y bueno. (Ver Figura 13)

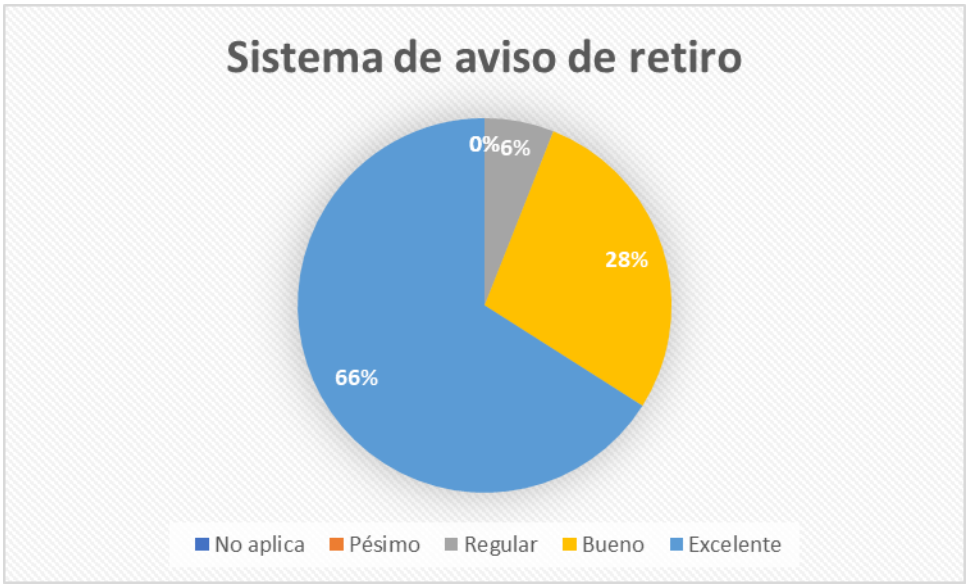


Figura 13. Grafica del Sistema de retiro de la Estación Automática.

- El control de servicio en la estación es del 95% entre excelente y bueno. (Ver Figura 14)

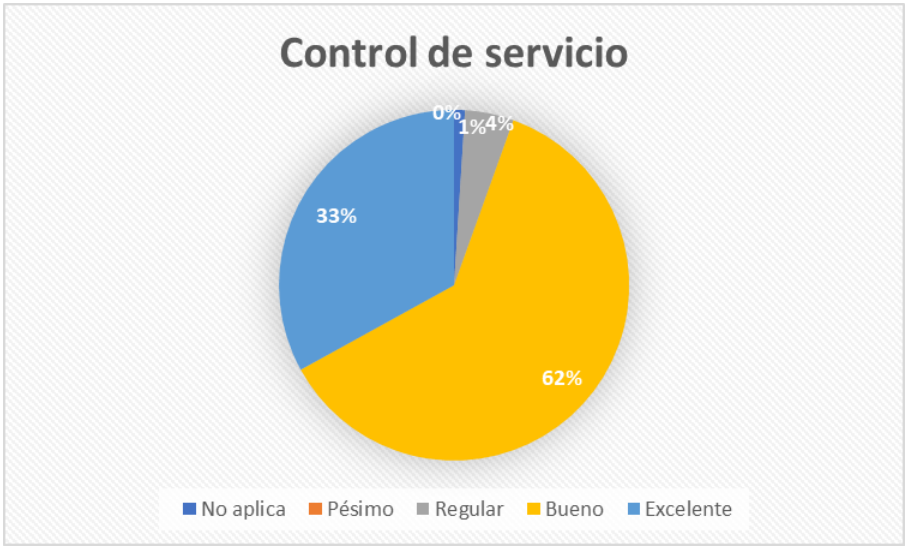


Figura 14.Grafica del Control de servicio en la estación.

-Plataforma Web:

En la Tabla 7 se presentan los resultados obtenidos en cuanto a la Plataforma Web del Sistema de Ecociclo.

PLATAFORMA						
	No aplica	Pésimo	Regular	Bueno	Excelente	TOTAL
Facilidad de interacción	0	0	36	130	34	200
Claridad en los procesos del servicio	0	2	38	123	37	200
Claridad de las interfaces y sus gráficos	0	0	47	115	38	200
Velocidad de respuesta de la plataforma	0	0	42	146	12	200
Sinergia de la estación y la plataforma	0	0	21	172	7	200
Presentación en general de la plataforma	0	0	6	183	11	200

Tabla 7. Resultados Obtenidos para la Plataforma Web del Sistema Ecociclo.

- La facilidad de interacción con la plataforma web del Sistema de Ecociclo es del 82% entre excelente y bueno. (Ver Figura 15)

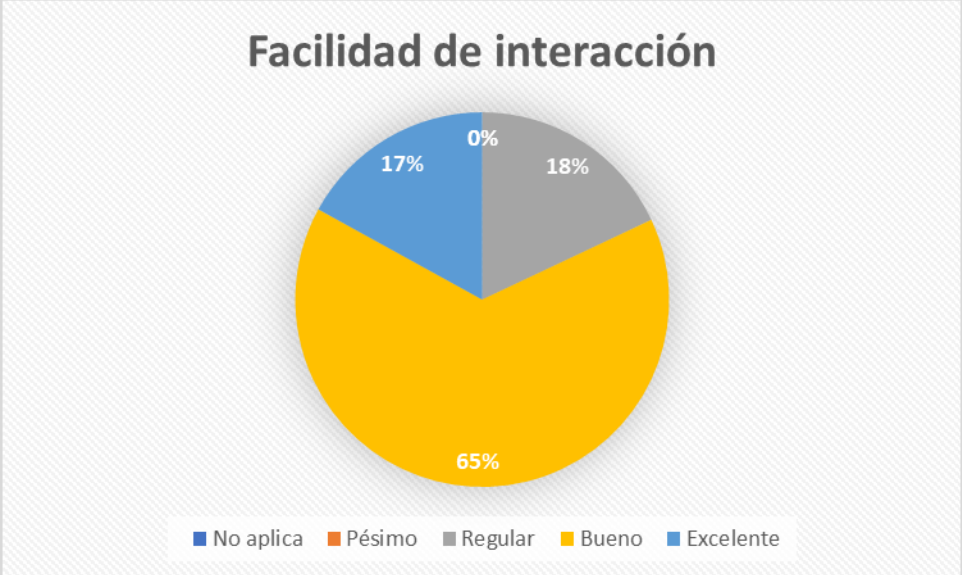


Figura 15.Grafica Facilidad de Interacción con la Plataforma Web.

- La claridad en los procesos del Servicio que expone la plataforma web del Sistema de Ecociclo es del 80% entre excelente y bueno. (Ver Figura 16)

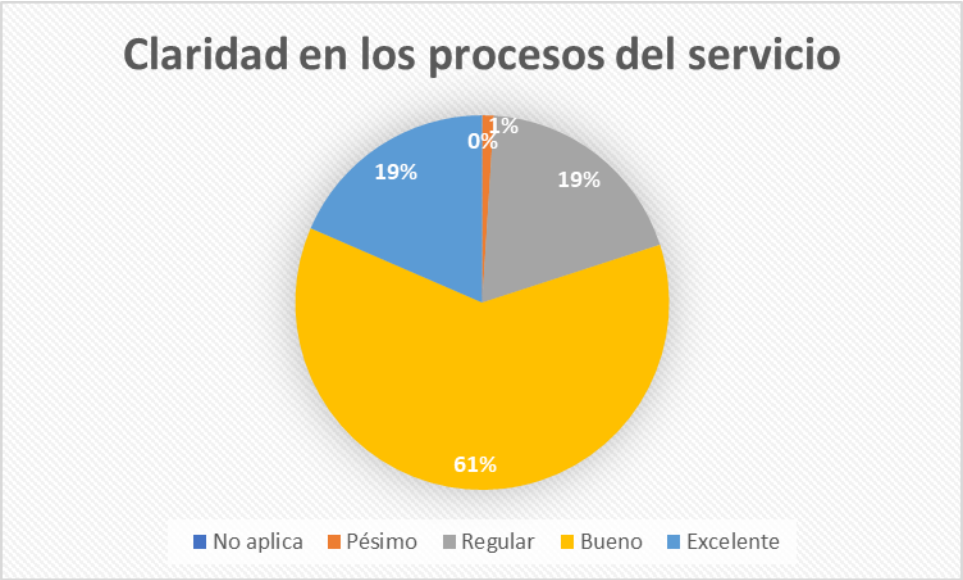


Figura 16.Grafica de la Claridad en los Procesos del Servicio a través de la Plataforma Web.

- La velocidad de la respuesta de la Plataforma Web del Sistema de Ecociclo es del 79% entre excelente y bueno. (Ver Figura 17).

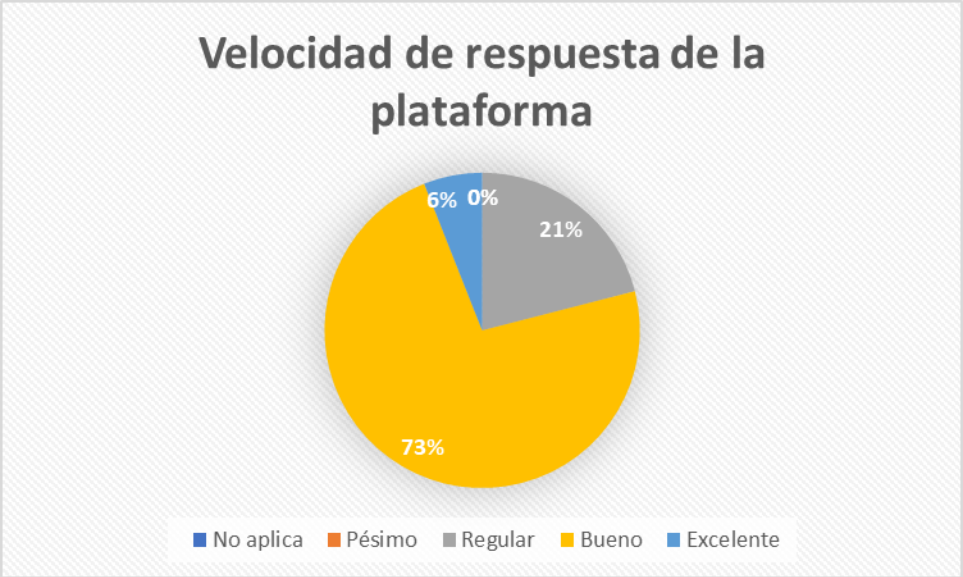


Figura 17.Grafica de la Velocidad de respuesta de la Plataforma Web.

- La claridad de las interfaces y los gráficos en la Plataforma Web del Sistema de Ecociclo es del 81% entre excelente y bueno. (Ver Figura 18).

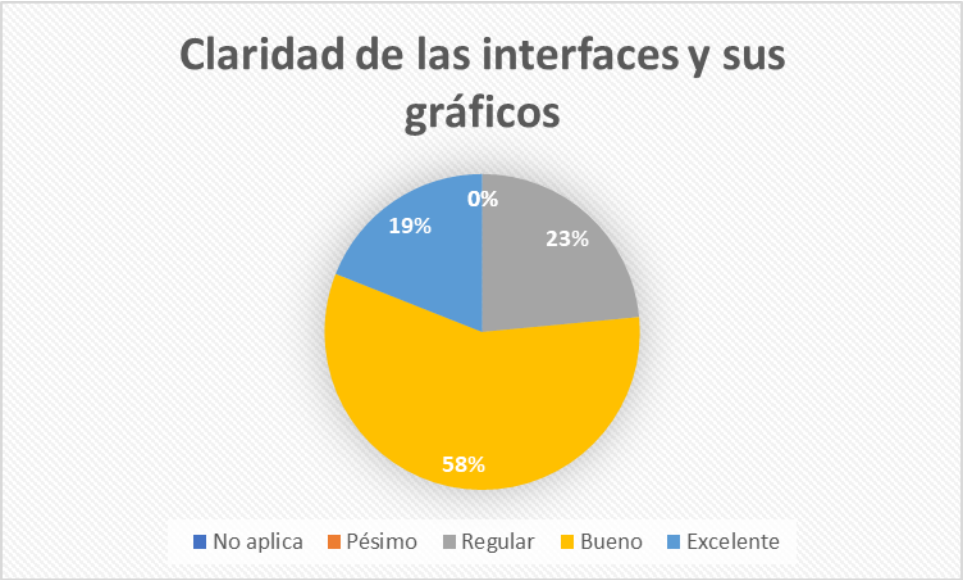


Figura 18.Grafica de la Claridad de las interfaces y sus graficas en la Plataforma Web.

- La presentación en general de la Plataforma Web del Sistema de Ecociclo es del 97% entre excelente y bueno. (Ver Figura 19).

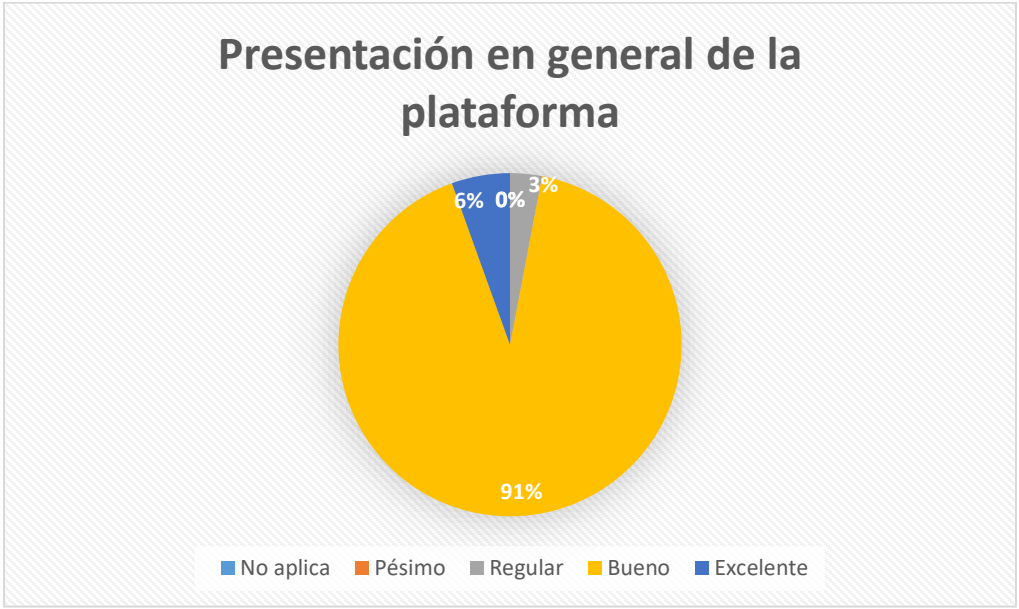


Figura 19.Grafica de la Presentación General de la Plataforma Web.

- La Sinergia de la Estación y la Plataforma Web del Sistema de Ecociclo es del 90% entre excelente y bueno. (Ver Figura 20).

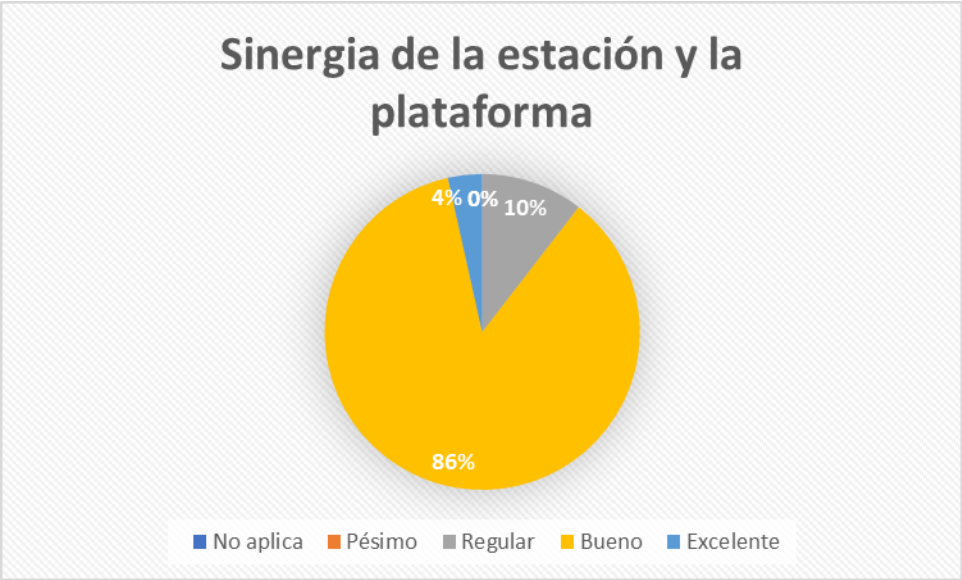


Figura 20.Sinergia de la estación y la Plataforma Web.

-Servicio:

En la Tabla 8 se presentan los resultados obtenidos en cuanto al Servicio del Sistema de Ecociclo.

SERVICIO						
	No aplica	Pésimo	Regular	Bueno	Excelente	TOTAL
Calidad del Servicio	0	0	64	136	34	200

Figura 21.Resultados obtenidos del Servicio del Sistema de Bicicletas Ecociclo.

- La calidad del Servicio del Sistema de Ecociclo es del 73% entre excelente y bueno. (Ver Figura 21).

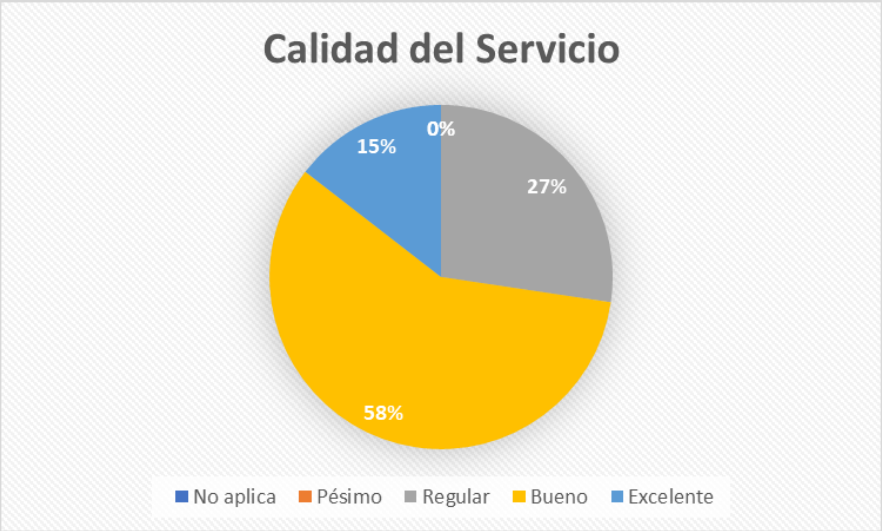


Figura 22.Grafica de la Calidad del Servicio del Sistema de Ecociclo.

-Conclusión:

La apreciación del Sistema en general es buena en los usuarios, aunque factores como Velocidad de respuesta, claridad en los procesos, en las interfaces y en la facilidad de interacción deben mejorar para aumentar la buena percepción de la plataforma web del mismo, en cuanto a la estación automática deben perfeccionarse el sistema de retiro y entrega de las bicicletas para facilitar estos procesos a los usuarios.